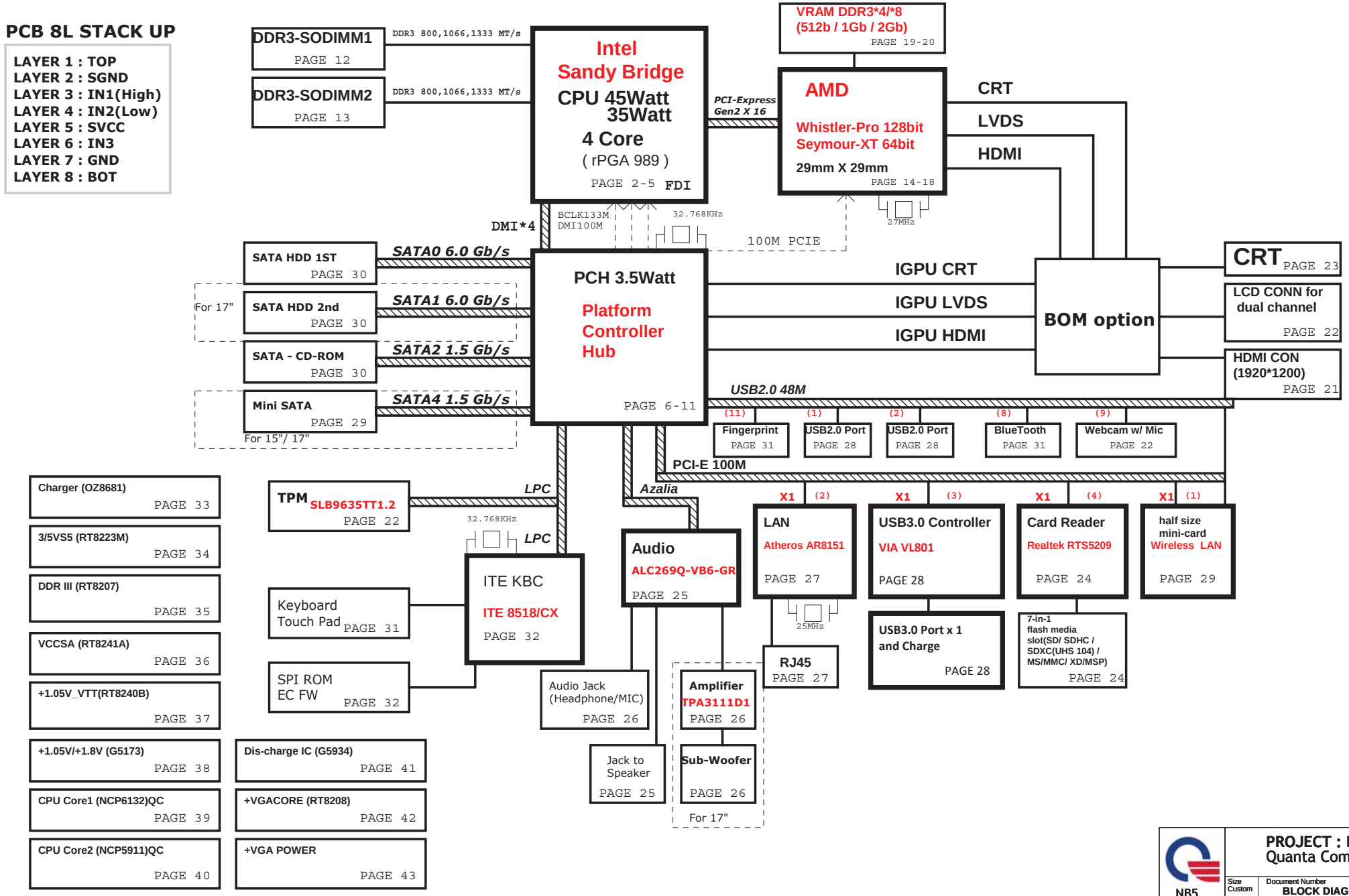
LG2/4 (14"/15.6") MUXLESS and Dis. BLOCK DIAGRAM 01

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT



NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	3A

Date: Wednesday, May 18, 2011 Sheet 1 of 47

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02

U25A

DMI

FDI Intel(R) FDI

eDP

PCI EXPRESS* - GRAPHICS

U25B

MISC

CLOCKS

THERMAL

DDR3 MISC

JTAG & BPM

PWR MANAGEMENT

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

SNB_IVB# N.A at SNB EDS #27637 0.7v1

Placement close to EC.

PROCTHOT# with two VR topology ..75ohm
PROCTHOT# with one VR topology ..56 ohm

R8219 Change to 25.5 ohm for intel DG.

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

CPU XDP

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

CPU RESET#

SM_DRAMPWROK Processor Input.

DDR3 DRAM RESET

FDI disable (DIS only stuff)

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

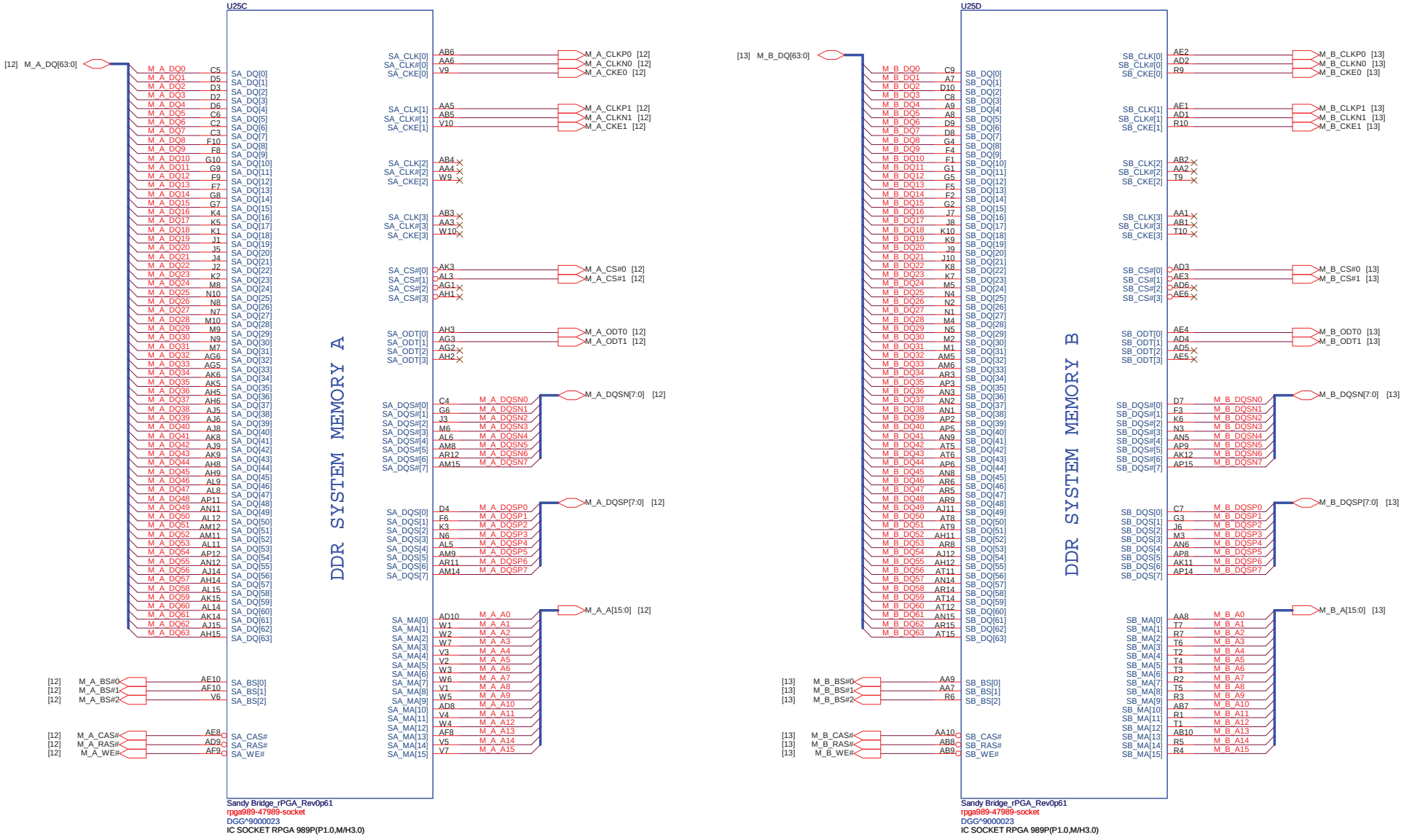
PROCTHOT# with two VR topology ..100ohm
PROCTHOT# with one VR topology ..62 ohm

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	3A
Date: Wednesday, May 18, 2011	Sheet 2 of 47	

Sandy Bridge Processor (DDR3)



NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	3A
Date: Wednesday, May 18, 2011	Sheet 3 of 47	

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04

U25F

SNB: 55A

+VCC_CORE

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

SNB: 8.5A

+1.05V_VTT

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

U25G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

SNB: 21.5A

+VCC_GFX

	DIS	Muxless/UMA
Ra	Stuff	NC

SNB: 1.5A

+1.8V

GRAPHICS

1.8V RAIL

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

MISC

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SNB: 5A

+1.5V_CPU

330uF x1, 10uF_8 x6 Socket BOT edge.

SNB: 6A

+VCCSA

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Add for intel CRB

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to VR

SVID CLK

SVID DATA

Place PU resistor close to CPU

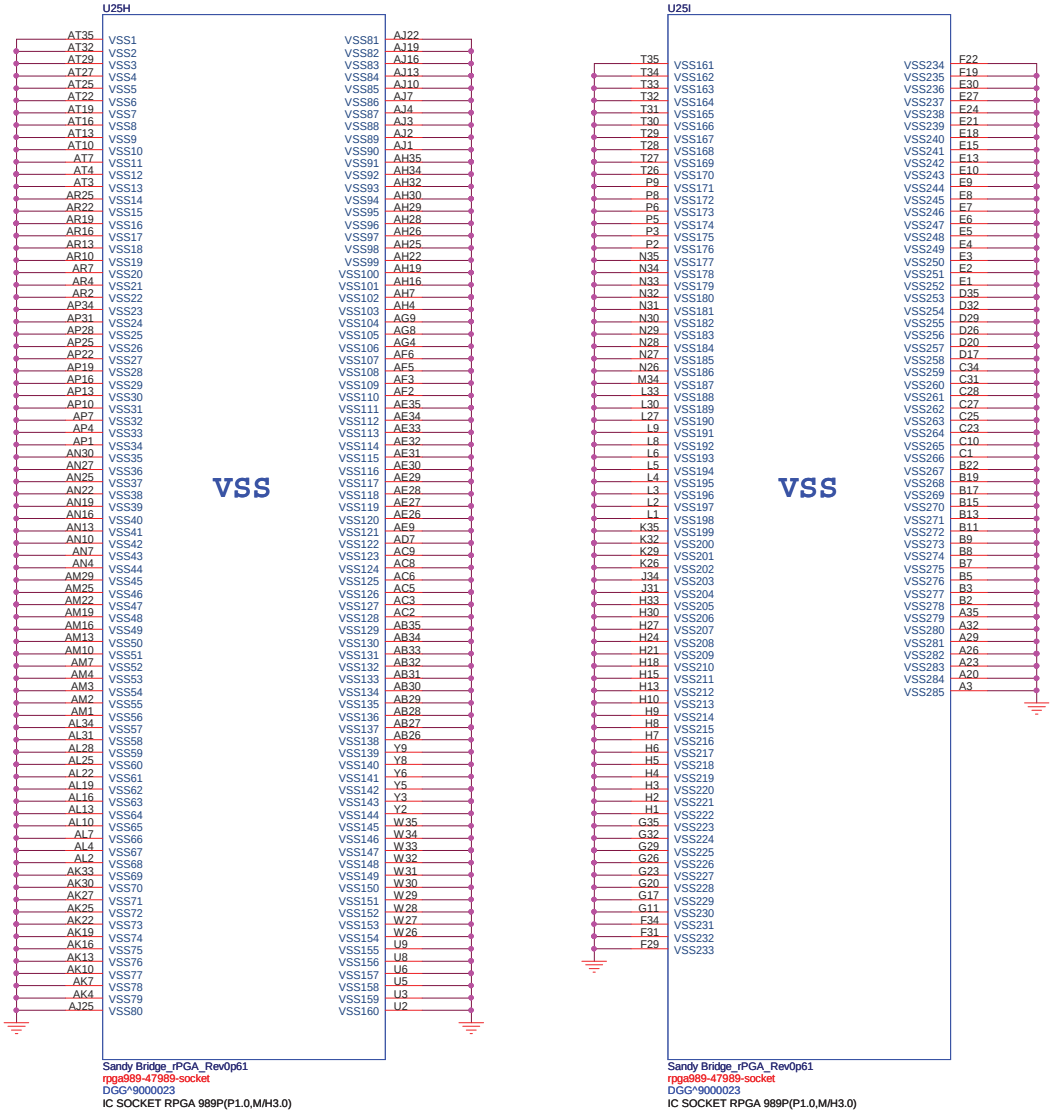
Place PU resistor close to CPU

SVID ALERT

CPU VDDQ

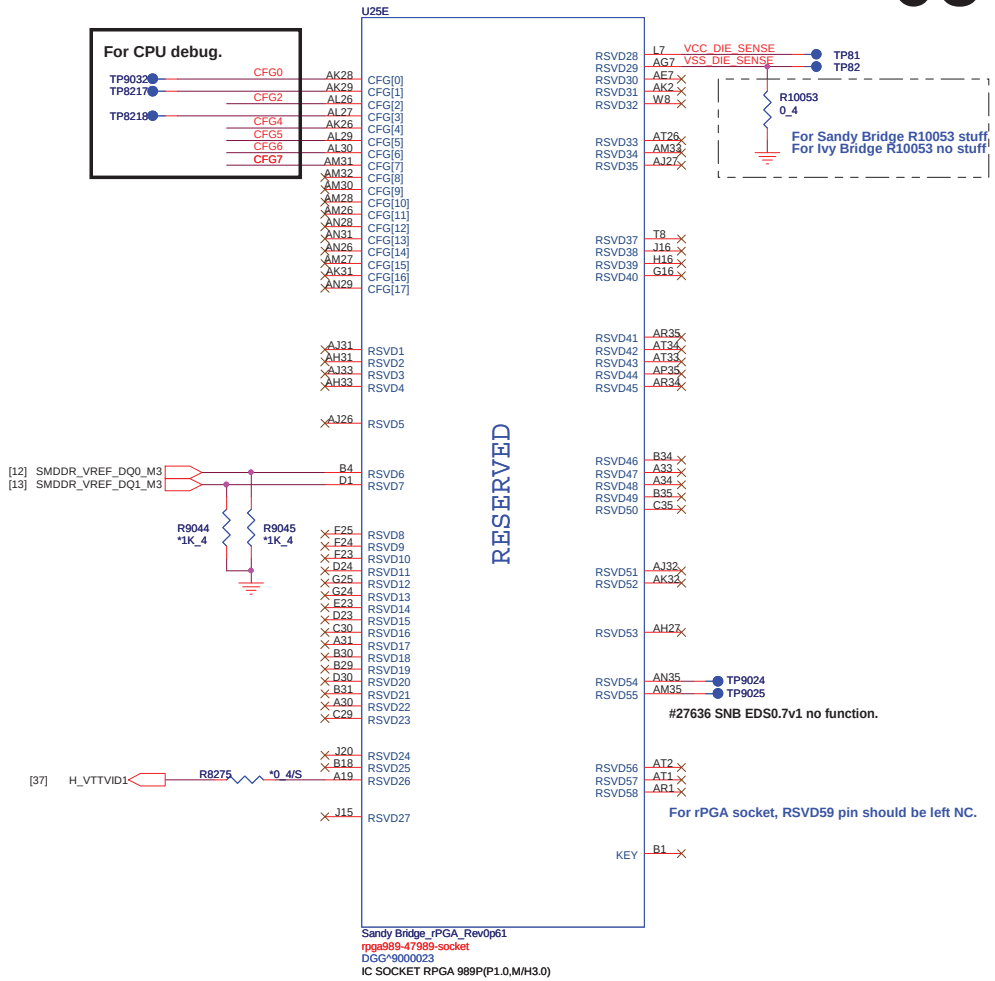
NB5	PROJECT : LG2/4 DIS Quanta Computer Inc.	
Size: Custom	Document Number: SNB 3/4 (POWER)	Rev: 3A
Date: Wednesday, May 18, 2011	Sheet 4 of 47	

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

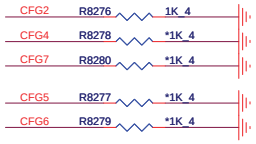
05



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

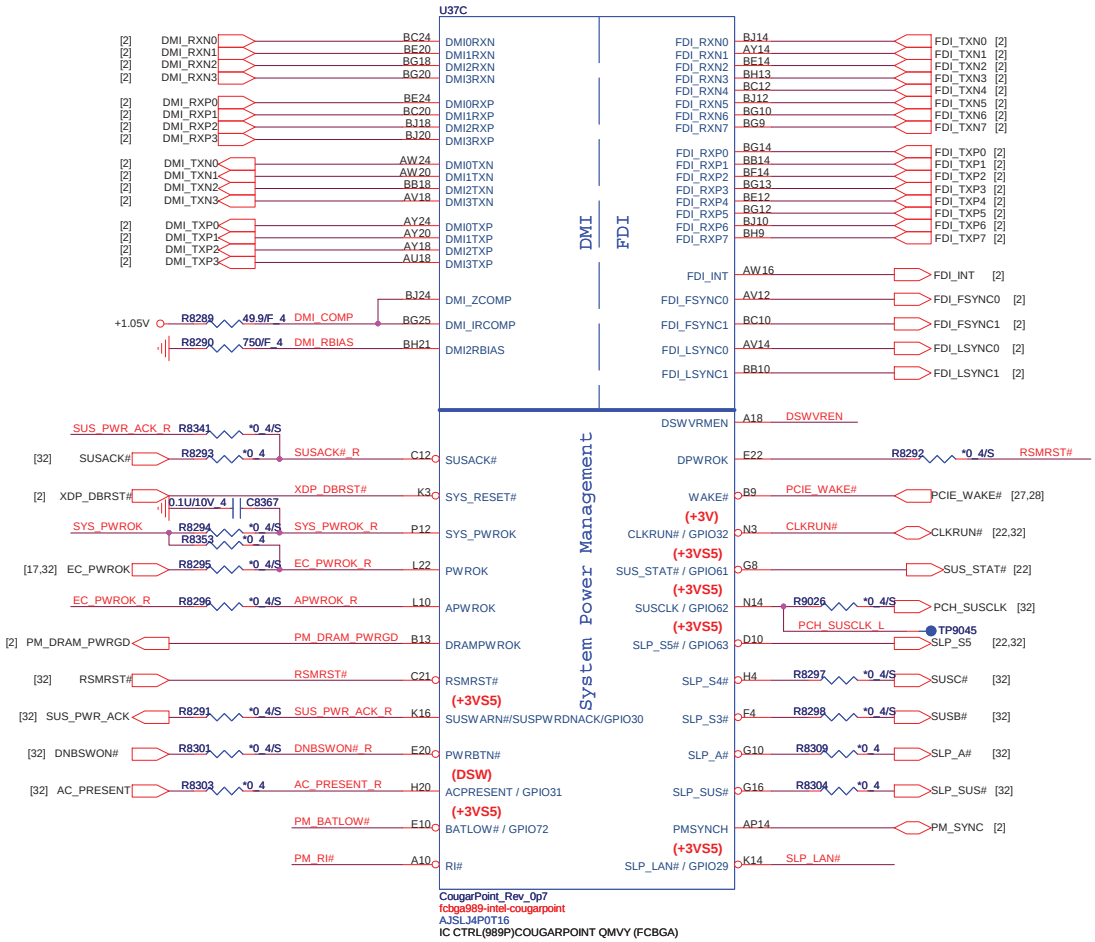
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

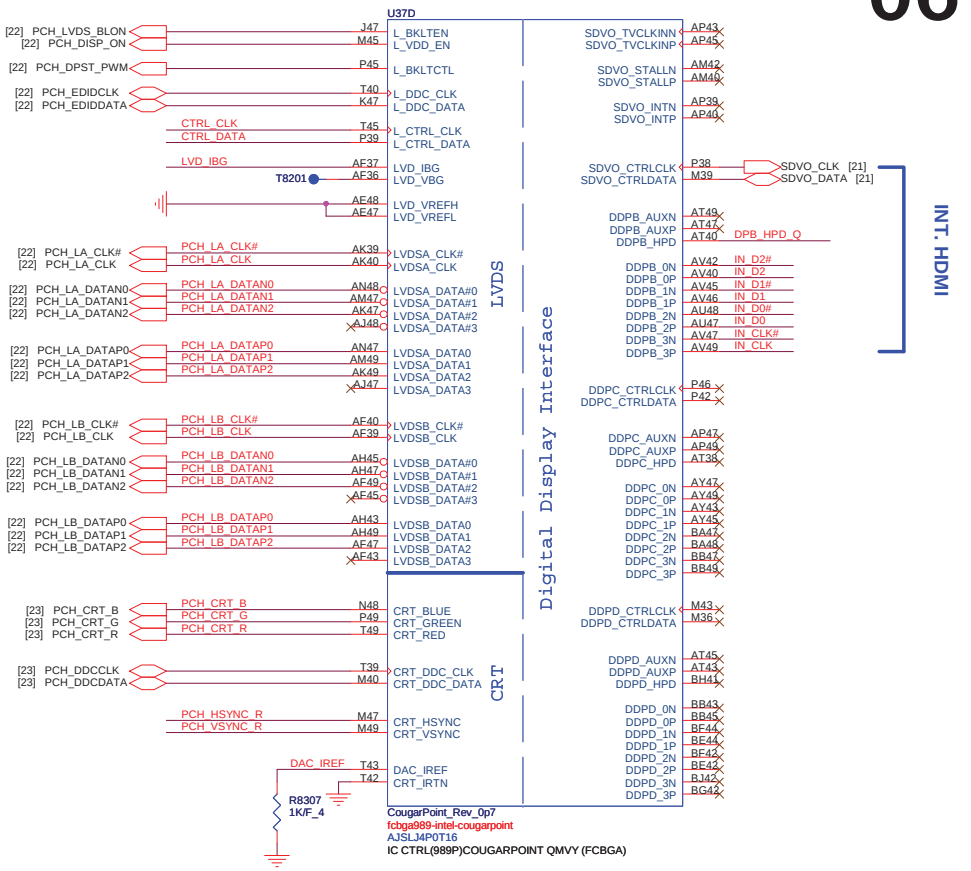
Size	Document Number	Rev
Custom	SNB 4/4 (GND)	3A

Date: Thursday, May 19, 2011 | Sheet 5 of 47

Cougar Point (DMI,FDI,PM)



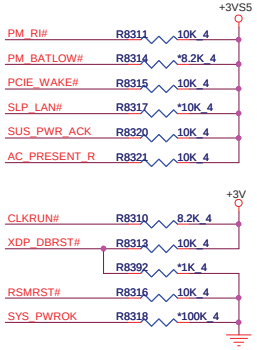
Cougar Point (LVDS,DDI)



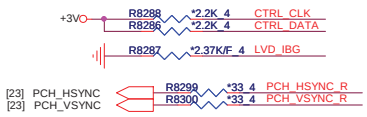
06

[7,10,17,21,22,23,25,29,30,31,41] +5V
[2,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
[2,7,8,9,10,27,29,32,34,37,38,41,43] +3VS5
[7,22,31,32,33,34] +3VPCU
[7,10,32] +3V_RTC
[2,4,7,8,10,28,32,37,38,39] +1.05V

PCH Pull-high/low(CLG)

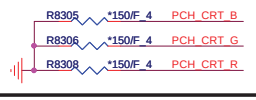


INT LVDS & CRT disable (DIS only remove)

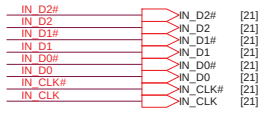


PD Res place close to PCH

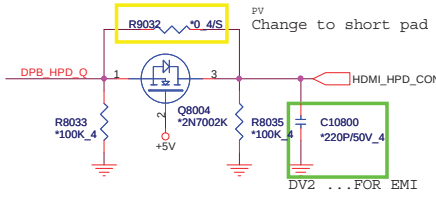
PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.



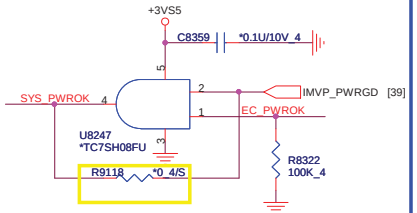
INT HDMI disable (DIS only remove)



INT HDMI Detect Function



System PWR_OK(CLG)



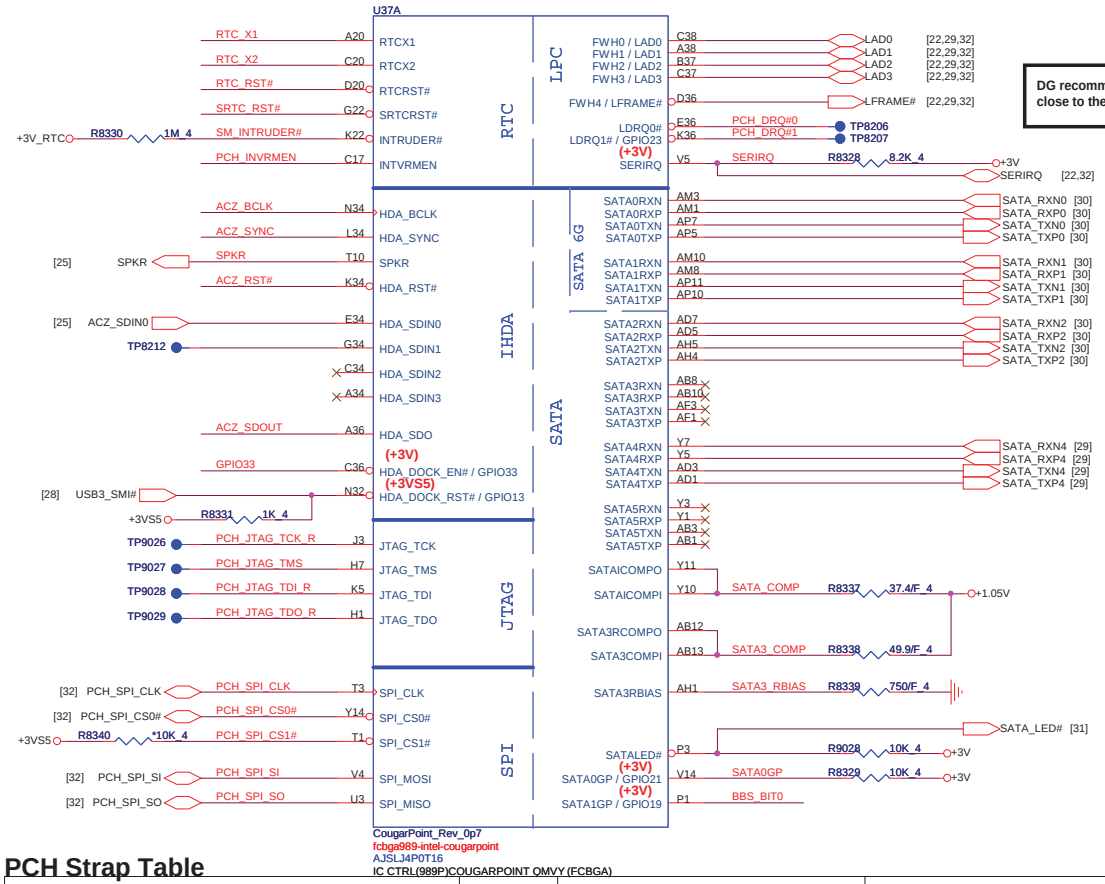
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	3A
Date: Wednesday, May 18, 2011	Sheet 6 of 47	

Cougar Point (HDA,JTAG,SATA)



CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJSLJ4P0T16
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

HDD0 (SATA3 6.0Gb/s)

2nd HDD0 (SATA3 6.0Gb/s)

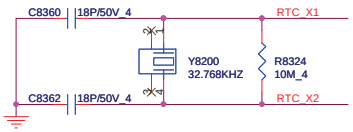
ODD

MINISATA (SATA1 1.5Gb/s)

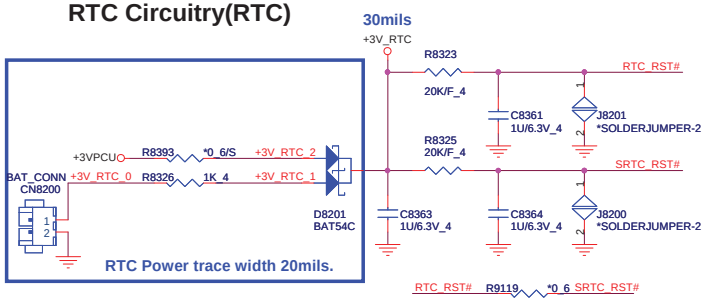
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R8349 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R8350 *1K_4 R9139 10K_4 PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R8351 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R8355 *1K_4 ACZ_SDOUT [32]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0; GNT0# 1 0; Boot Location SPI LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		BBS_BIT0 R8358 *1K_4 R8357 *1K_4 BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R8359 *1K_4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R8360 2.2K_4 R8361 1K_4 NV_CLE [8] H_SNB_IVB# [2]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R9146 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	[32] ACZ_SDOUT ACZ_SDOUT R8362 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R8365 *1K_4 ICC_EN# [9]
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R8366 *1K_4 PLL_ODVR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R8398 1K_4 +3V

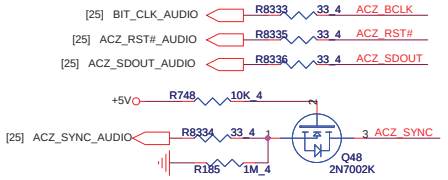
RTC Clock 32.768KHz



RTC Circuitry(RTC)



HDA Bus(CLG)



[10] +V3.3A_1.5A_HDA_IO
[6,10,17,21,22,23,25,29,30,31,41] +5V
[2,6,8,9,10,27,29,32,34,37,38,41,43] +3VS5
[22,31,32,33,34] +3VPCU
[2,6,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V

[6,10,32] +3V_RTC
[4,10,38] +1.8V
[2,4,6,8,10,28,32,37,38,39] +1.05V

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	3A

Date: Thursday, May 19, 2011 Sheet 7 of 47

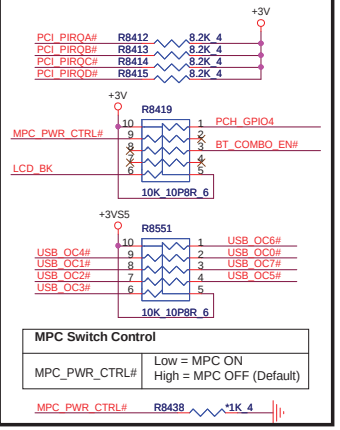
07

08

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

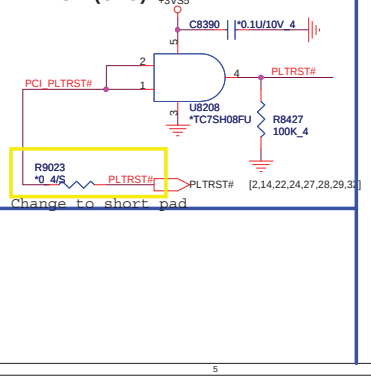
PCI/USBOC# Pull-up(CLG)



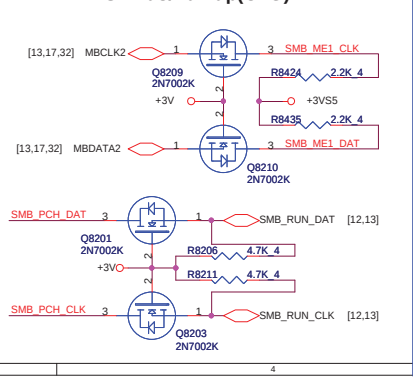
MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R8438 *1K_4

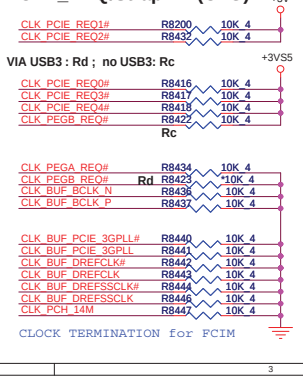
PLTRST#(CLG)



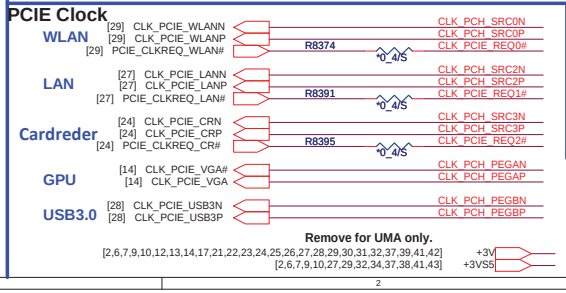
SMBus/Pull-up(CLG)



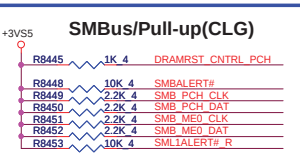
CLK_REQ/Strap Pin(CLG)



PCIE Clock



SMBus/Pull-up(CLG)



DV2

Add Board_ID6, Board_ID7
FOR CB Project

8/23 A-->B update.

HM65 Port6 & Port7 are disable

USBP1- [31] USBP1+ [31]	Right_USB 15"
USBP2- [31] USBP2+ [31]	Right_USB 15"
USBP4- [28] USBP4+ [28]	USB
USBP8- [31] USBP8+ [31]	Blue tooth
USBP9- [22] USBP9+ [22]	Webcam
USBP10- [29] USBP10+ [29]	MinPCIE-USB-H
USBP11- [31] USBP11+ [31]	Fingerprint

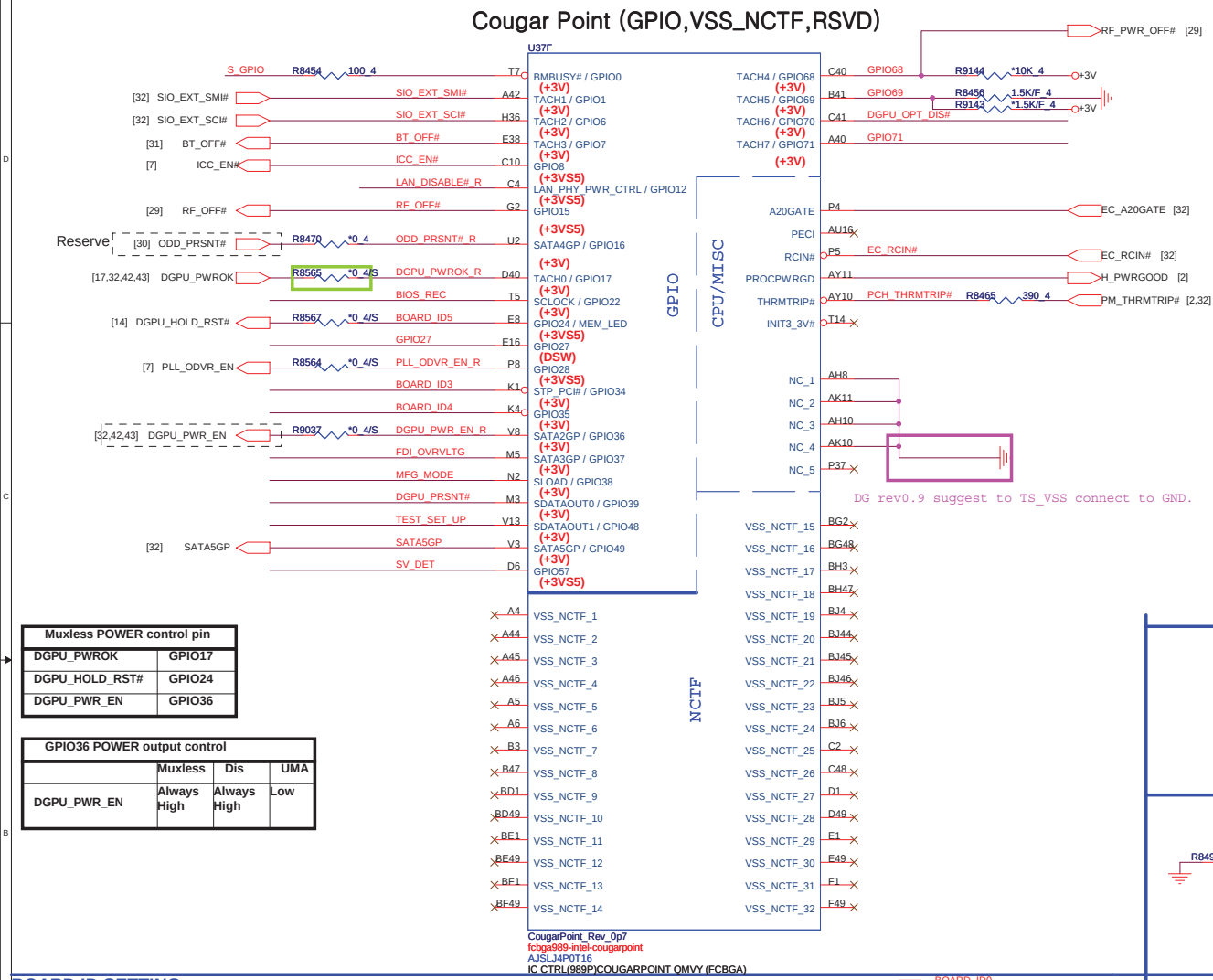
CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJSLJ4P0T16
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJSLJ4P0T16
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

Project	PROJECT : LG2/4 DIS Quanta Computer Inc.
Size / Custom	Document Number: PCH 3/6 (PCIE/USB/CLK)
Rev	3A
Date: Thursday, May 19, 2011	Sheet 8 of 47

NB5

Cougar Point (GPIO,VSS_NCTF,RSVD)

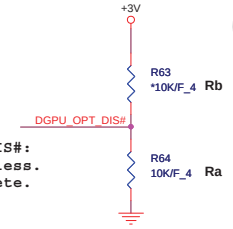


Muxless POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

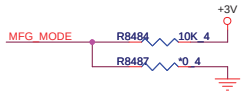
GPIO36 POWER output control			
	Muxless	Dis	UMA
DGPU_PWR_EN	Always High	Always High	Low

	Ra	Rb
UMA/Muxless	NC	Stuff
DIS	Stuff	NC

DGPU_OPT_DIS#:
High : Muxless.
Low: Discrete.

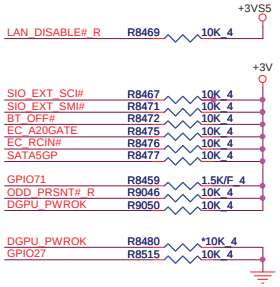


MFG-TEST



SGPIO

GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

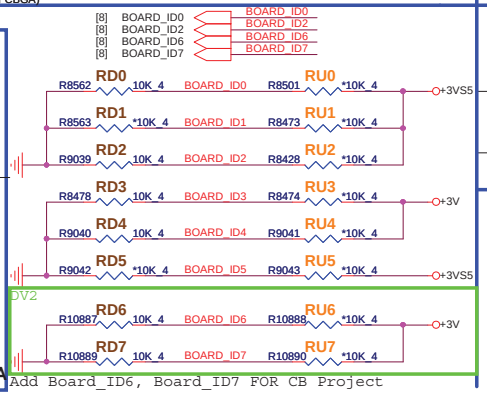
BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

TEST DETECT
Low = Default

BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID6	ID7	GPIO70	GPIO39
LG/CB	0=LG 1=CB								
15.6"/ 14"			ID2 1	14" 1	15" 0	17" 0	LG6 1		
17"			ID3 0	0	1	1			
dobly					1=YES 0=NO				
DIS/Muxless								1= Muxless 0=DIS	
UMA/VGA									1= VGA 0=UMA

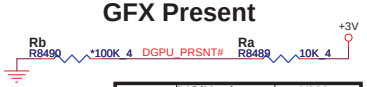


Add Board_ID6, Board_ID7 FOR CB Project

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

GFX Present



	DIS/Muxless	UMA
Stuff	Ra	Rb
NC	Rb	Ra

[2,6,7,8,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42]
[2,6,7,8,10,27,29,32,34,37,38,41,43]
+3V
+3VS5

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	3A
Date: Wednesday, May 18, 2011	Sheet 9 of 47	

Cougar Point-M (POWER)

COUGAR POINT (POWER)

U37J

Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA

U37G

VCC CORE
CRT
LVDS
HVCMOS
VCCIO
DMI
SPI
NAND / SPI
FDI

Near PCH

1.3 A (60mils)
2.925 A (140mils)
1.01A (60mils)
119mA (20mils)
119mA (15mils)
266mA (20mils)
160mA (20mils)
65mA (10mils)
8mA (10mils)
55mA (10mils)
95mA (10mils)
3mA (10mils)
V_PROC_IO=1mA (10mils)
VCCRTC<1mA (10mils)
20mA (10mils)
1mA (10mils)
60mA (10mils)
42mA (10mils)
190 mA (15mils)
160mA (15mils) (Mobile 1.5V)
VCC5REFSUS=1mA
V5REF= 1mA
10mA (10mils)
65mA (10mils)
8mA (10mils)

PV
Change to short pad

DV2 add for +5V_S5 leakage issue

Muxless : Ra
UMA : Ra
DIS : Rb

UMA & Muxless Only, If have power noise issue then stuff it.

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJSLJ4P0T16
IC CTRL(989P)COUGARPOINT QMVY (FCBGA)

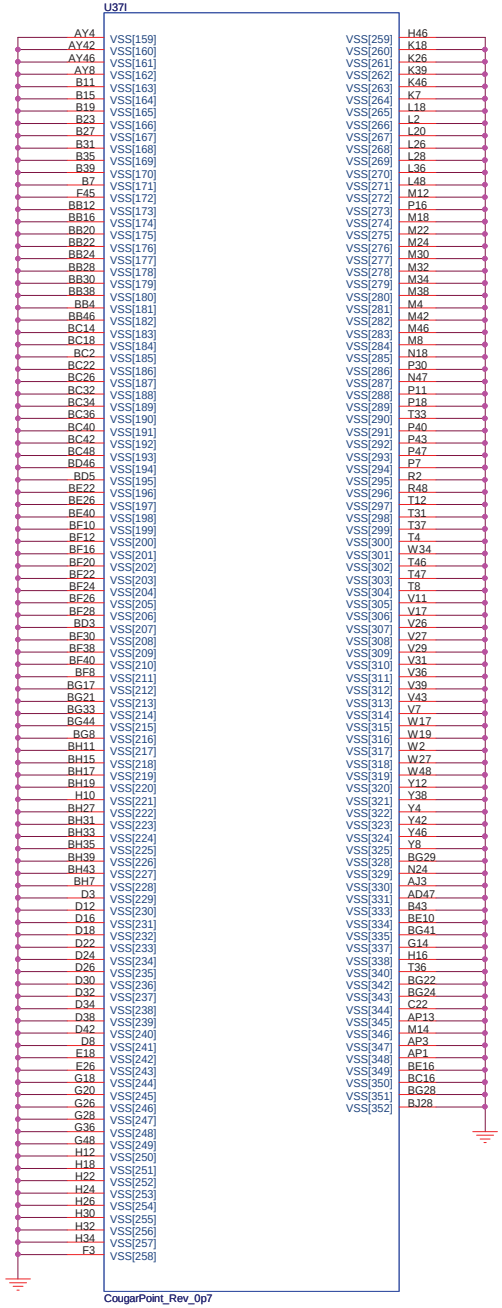
PROJECT : LG2/4 DIS
Quanta Computer Inc.

NB5

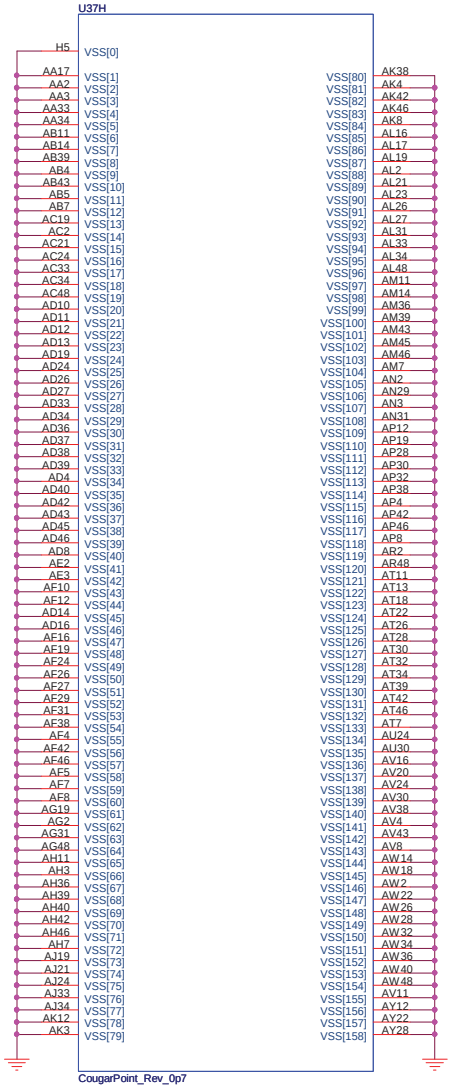
Size: Custom | Document Number: PCH 5/6 (POWER) | Rev: 3A

Date: Wednesday, May 18, 2011 | Sheet 10 of 47

IBEX PEAK-M (GND)



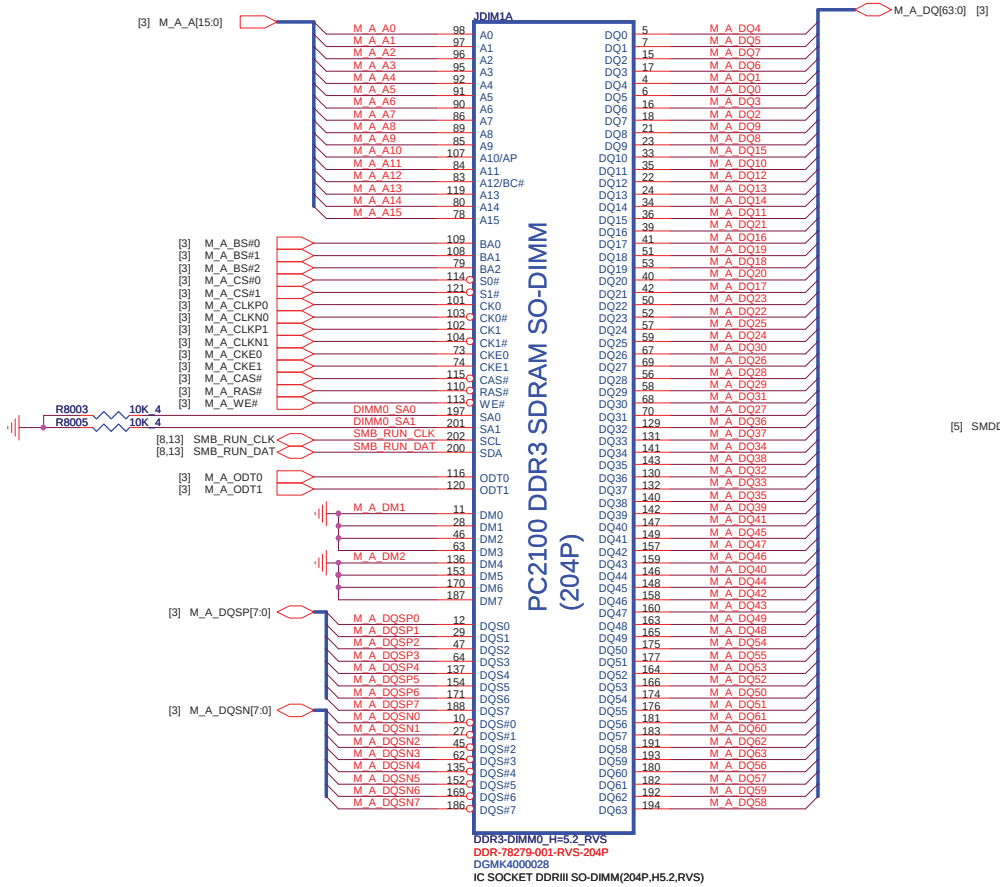
IBEX PEAK-M (GND)

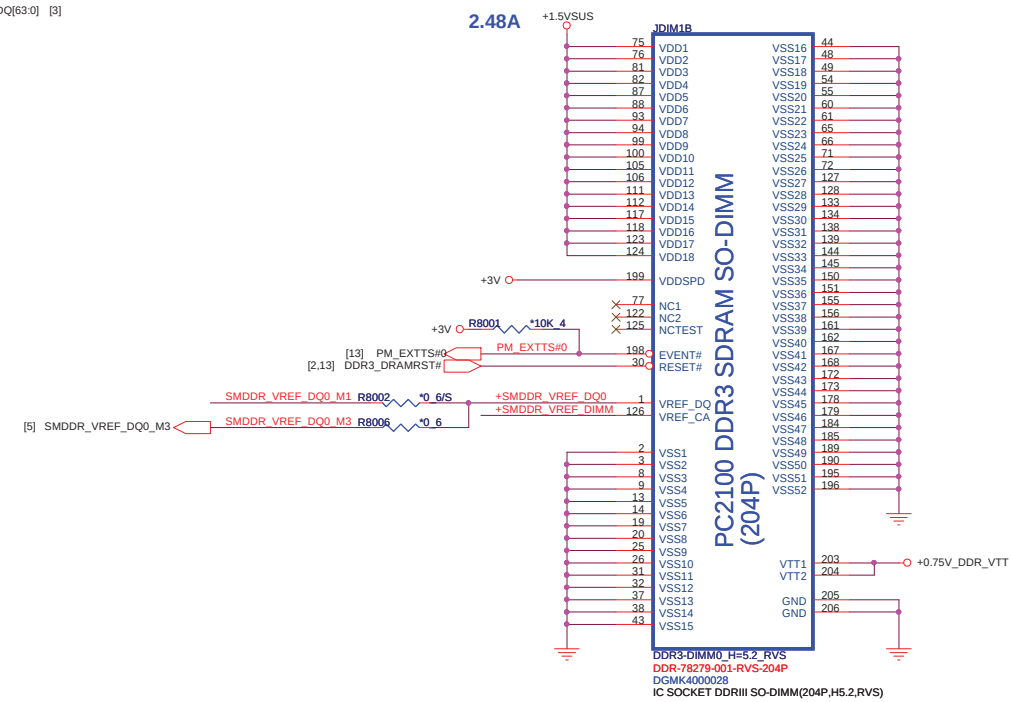


NB5

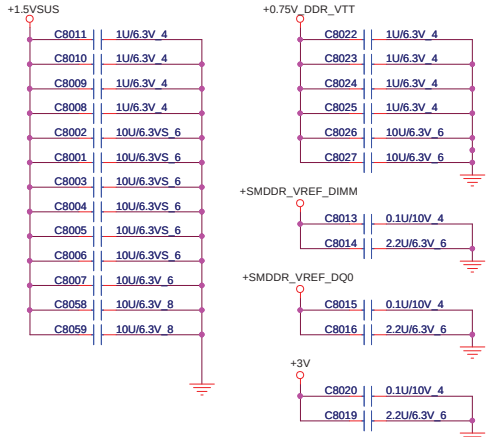
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	3A
Date: Wednesday, May 18, 2011	Sheet 11 of 47	

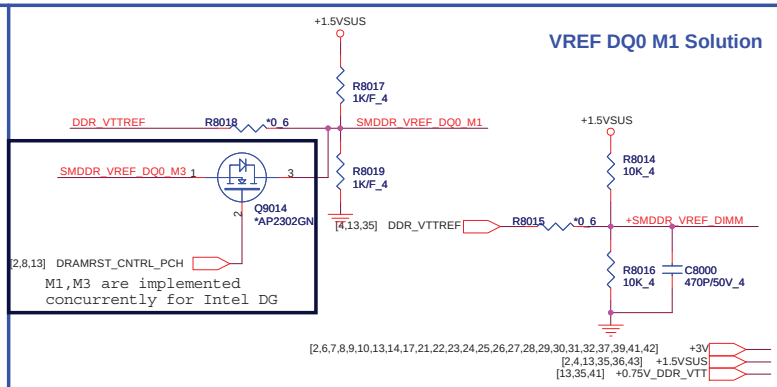




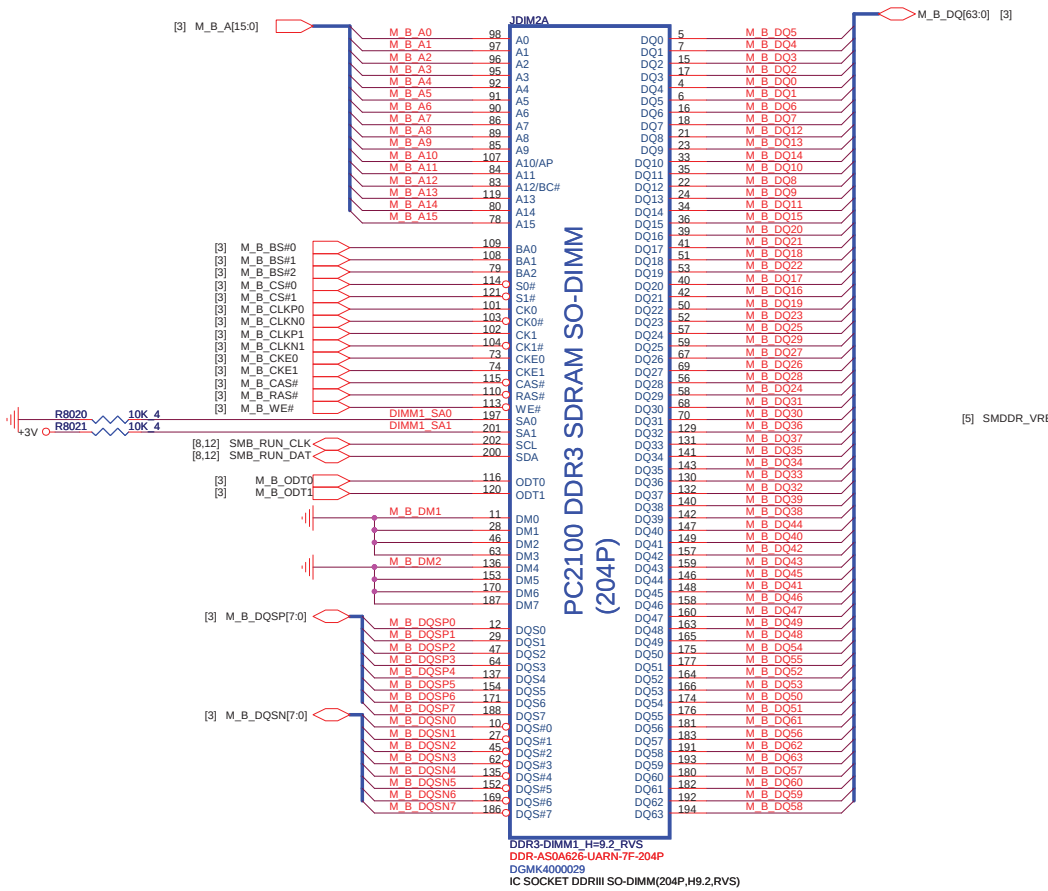
Place these Caps near So-Dimm0.

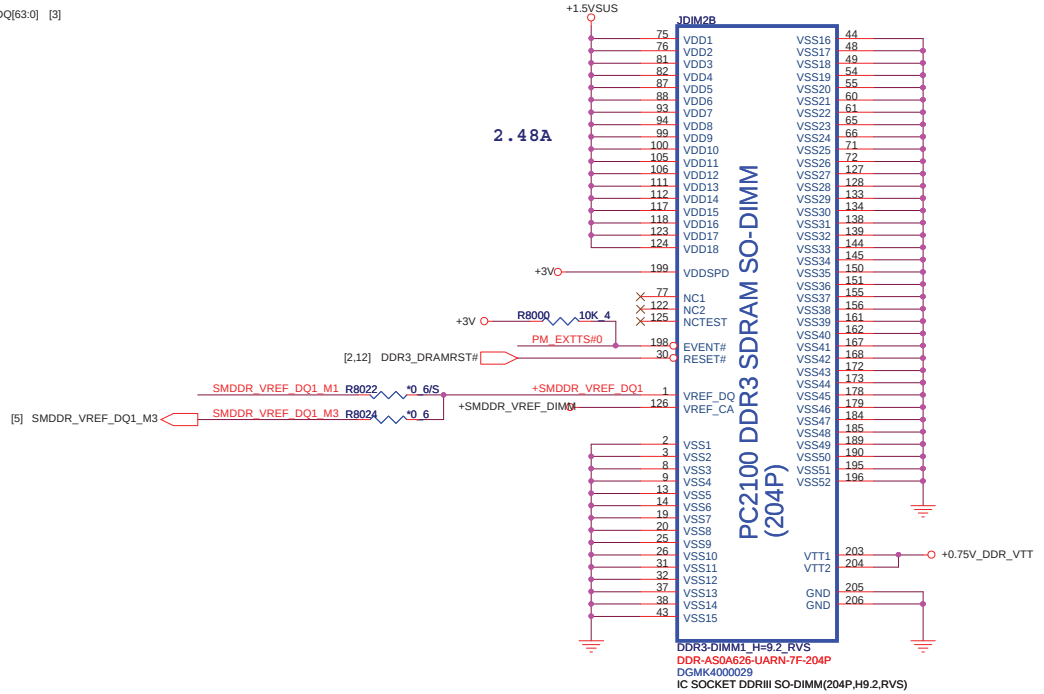


VREF DQ0 M1 Solution

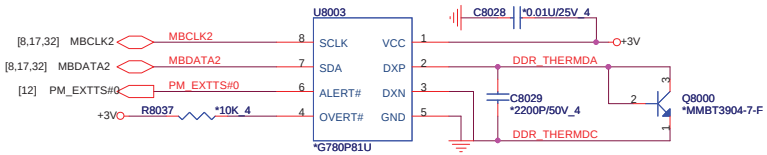


NB5	PROJECT : LG2/4 DIS Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM0-RVS (5.2H)	Rev: 3A
Date: Wednesday, May 18, 2011	Sheet 12 of 47	

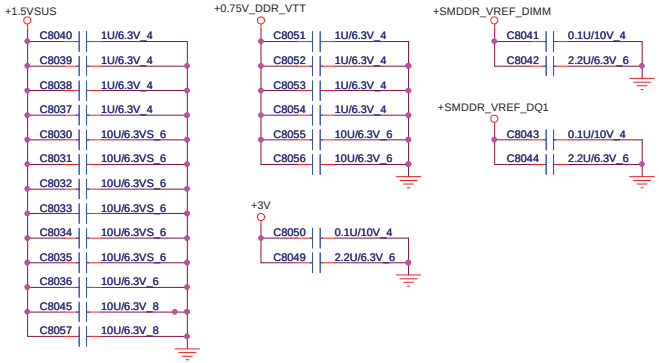




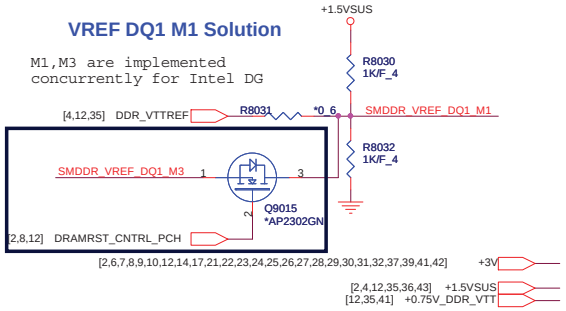
DDR3 Thermal Sensor



Place these Caps near So-Dimm1.



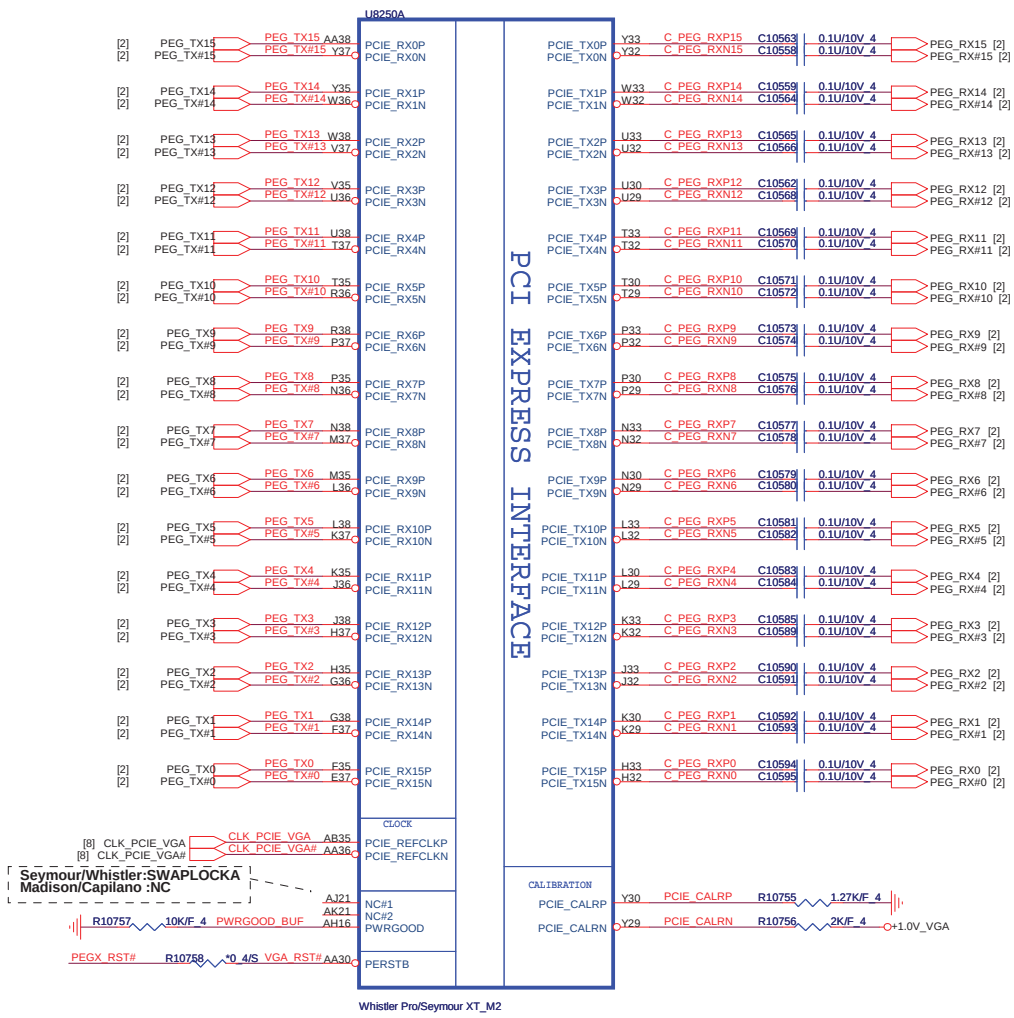
VREF DQ1 M1 Solution

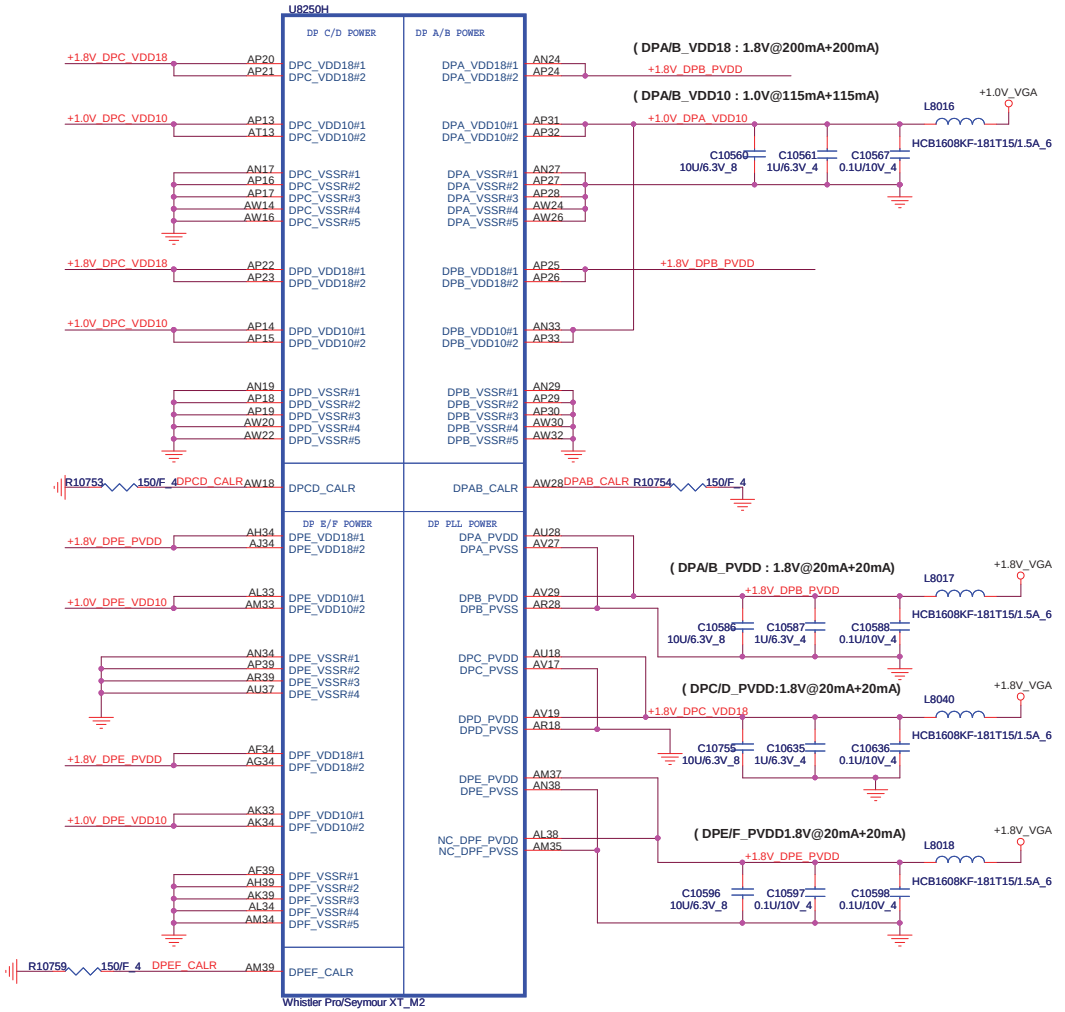


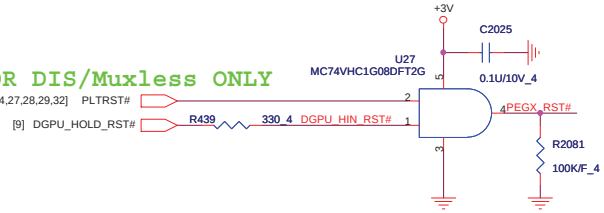
NB5

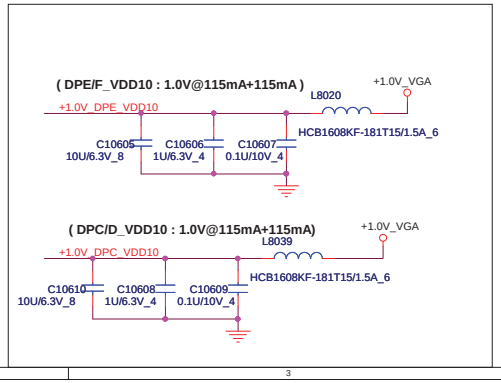
PROJECT : LG2/4 DIS
Quanta Computer Inc.

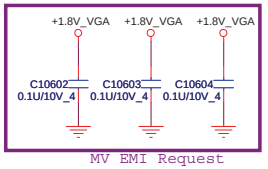
Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	3A
Date: Wednesday, May 18, 2011	Sheet 13 of 47	











[2,6,7,8,9,10,12,13,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
[16,18,43] +1.8V_VGA
[16,17,18,43] +1.0V_VGA

NB5

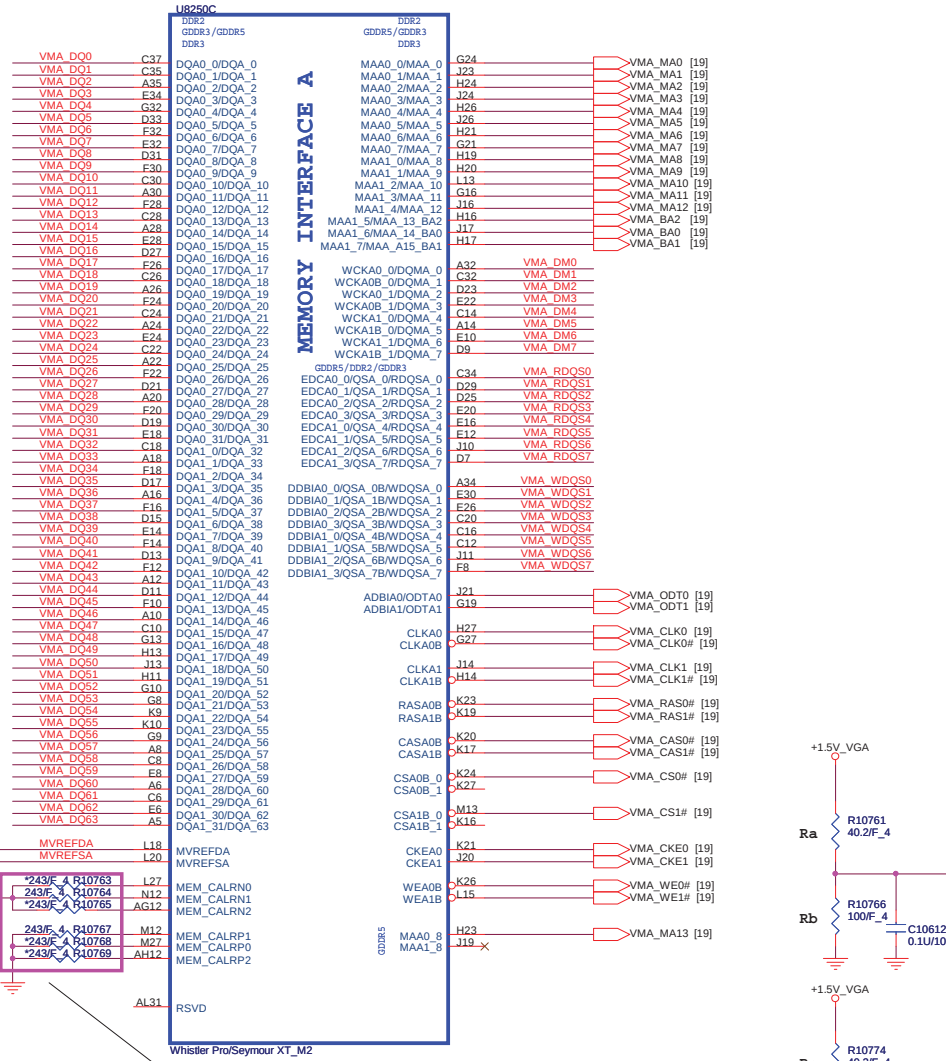
PROJECT : LG2/4 DIS
Quanta Computer Inc.

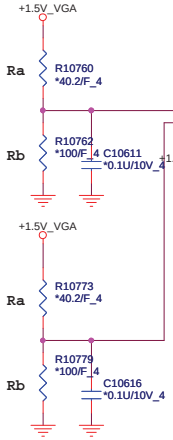
Size	Document Number	Rev
Custom	AMD Whistler (MEM)1/5	3A

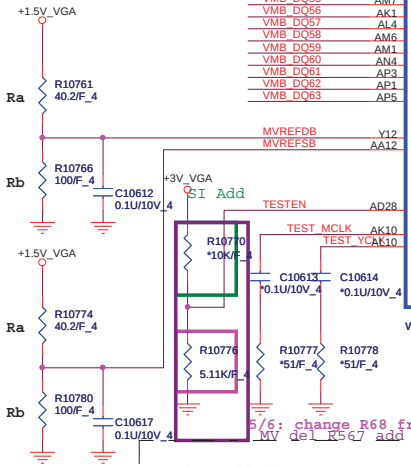
Date: Wednesday, May 18, 2011 Sheet 14 of 47

Seymour Use Channel B Memory Interface Only

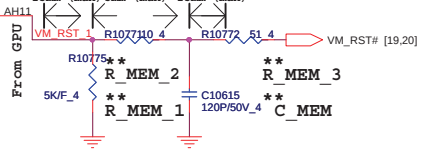
[19] VMA_DQ[63..0]
[19] VMA_DM[7..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]
[20] VMB_DQ[63..0]
[20] VMB_DM[7..0]
[20] VMB_WDQS[7..0]
[20] VMB_RDQS[7..0]







5/6: change R68 from 10k to 5.11k for AMD
_MV del R567 add R68 in BOM



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

[18,19,20,43] +1.5V_VGA

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

	For Whistler	For Seymour
MEM_CALRNP0	stuff	NC
MEM_CALRNP1	stuff	stuff
MEM_CALRNP2	stuff	NC
MVREFDA	stuff	NC
MVREFSA	stuff	NC

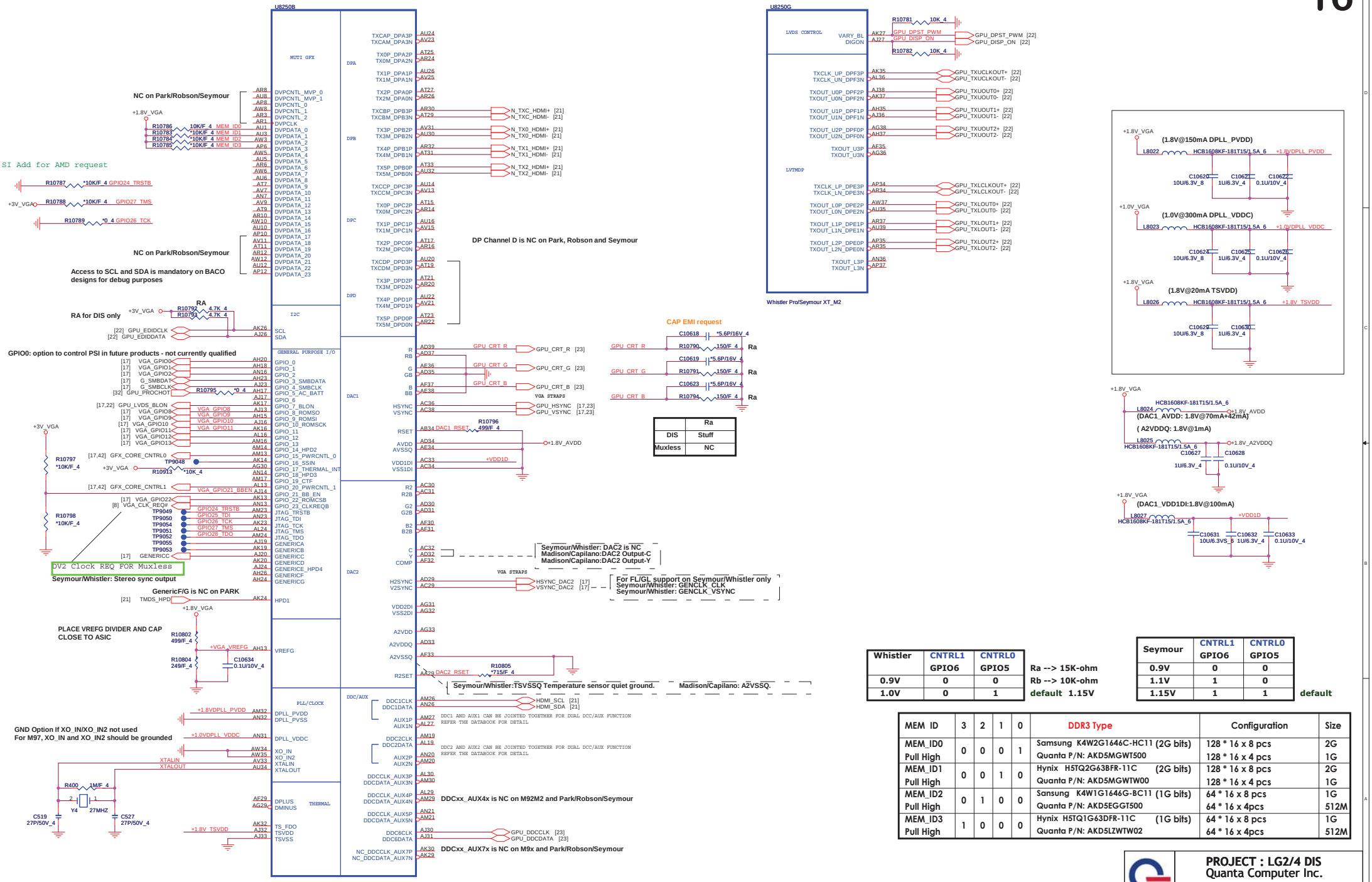
Designator	
R_MEM_1	5K
R_MEM_2	10R
R_MEM_3	51R
C_MEM	120pF

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD Whistler (MEM)2/5	3A

Date: Wednesday, May 18, 2011 Sheet 15 of 47



Whistler	CNTRL1 GPIO6	CNTRL0 GPIO5
0.9V	0	0
1.0V	0	1

Ra --> 15K-ohm
Rb --> 10K-ohm
default 1.15V

Seymour	CNTRL1 GPIO6	CNTRL0 GPIO5
0.9V	0	0
1.1V	1	0
1.15V	1	1

default

	Ra
DIS	Stuff
Muxless	NC

MEM_ID	3	2	1	0	DDR3 Type	Configuration	Size
MEM_ID0	0	0	0	1	Samsung K4W2G1646C-HC11 (2G bits)	128 * 16 x 8 pcs	2G
Pull High					Quanta P/N: AKD5MGWT500	128 * 16 x 4 pcs	1G
MEM_ID1	0	0	1	0	Hynix H5TQ2G63BFR-11C (2G bits)	128 * 16 x 8 pcs	2G
Pull High					Quanta P/N: AKD5MGWTW00	128 * 16 x 4 pcs	1G
MEM_ID2	0	1	0	0	Sansung K4W1G1646G-BC11 (1G bits)	64 * 16 x 8 pcs	1G
Pull High					Quanta P/N: AKD5EGGT500	64 * 16 x 4pcs	512M
MEM_ID3	1	0	0	0	Hynix H5TQ1G63DFR-11C (1G bits)	64 * 16 x 8 pcs	1G
Pull High					Quanta P/N: AKD5LZWTW02	64 * 16 x 4pcs	512M

[14,17,18,43] +1.0V_VGA
[14,18,43] +1.8V_VGA
[15] +3V_VGA

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD Whistler DISPLAY3/5	3A

Date: Thursday, May 19, 2011 Sheet 16 of 47

STRAPS

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

DV2 Change R10806 non stuff

+3V_VGA

[16] VGA_GPIO0	R10806	*10K/F_4	
[16] VGA_GPIO1	R10807	*10K/F_4	
[16] VGA_GPIO2	R10808	*10K/F_4	
[16] VGA_GPIO8	R10809	*10K/F_4	
[16] VGA_GPIO9	R10810	*10K/F_4	
[16] VGA_GPIO13	R10811	10K/F_4	
	R10812	*10K/F_4	
[16] VGA_GPIO12	R10813	10K/F_4	
	R10814	*10K/F_4	
[16] VGA_GPIO11	R10815	*10K/F_4	
	R10816	10K/F_4	
[16] VGA_GPIO10	R10817	*10K/F_4	GPIO10 for EEPROM.
[16] GENERICC	R10818	*10K/F_4	
[16] VGA_GPIO22	R10819	*10K/F_4	GPIO22 for Enable EEPROM
[16,23] GPU_VSYNC	R10827	*10K/F_4	Re
	R10820	10K/F_4	Rf
[16,23] GPU_HSYNC	R10828	*10K/F_4	Rg
	R10821	10K/F_4	Rh
[16] VSYNC_DAC2	R10822	*10K/F_4	
[16] HSYNC_DAC2	R10823	*10K/F_4	
[16,22] GPU_LVDS_BLON	R10824	10K/F_4	
[16,42] GFX_CORE_CNTRL0	R10825	*3K/F_4	
[16,42] GFX_CORE_CNTRL1	R10826	*3K/F_4	

	Re	Rf	Rg	Rh
PX4.0	Stuff	NC	Stuff	NC
Discrete	NC	Stuff	NC	Stuff

Reserve for support BACO mode

Rb

PX_EN_1 — R10829 0_4 — PX_EN

	Ra	Rb
BACO Functions	Stuff	Stuff 5.1k
NO BACO Functions	NC	Stuff 0 ohm

Ra

Support BACO Mode : Stuff All Location
NO Support BACO Mode : No Stuff All Location

PX_MODE=1, for Normal Operation (Default)
PX_MODE=0, for BACO MODE

PX_EN=1, for BACO MODE
PX_EN=0, for Normal Operation (Default)

C889 *0.1U/10V_4 — [9,32,42,43] DGPU_PWROK — PX_MODE — U40 *TC7SH08FU — BACO_EN

R10865 *100K/F_4 — Q9016 *2N7002 — Q9017 *2N7002 — PX_EN# — [6,32] EC_PWROK — [42] PX_MODE

Q9009 *2N7002 — PX_EN

R10838 *1K_4 — Q9007 *2N7002 — PX_EN#2

R10839 *1K_4 — Q9008 *2N7002 — PX_EN##

[43] PX_MODE1 — Q9018 *2N7002 — PX_EN

+1.0V_VGA — Q9010 *AO3404 — Q9012 *AO3404 — PX_EN#

+VGACORE — Q9011 *AO3404 — Q9013 *AO3404 — PX_EN##

BIF_VDDC — C10729 *22U/6.3VS_8

GFx SMBus Isolation

[16] G_SMBCLK — R481 4.7K_4 — Q55 2N7002 — MBCLK2 [8,13,32]

+3V_VGA — DV2 Change to +3V_VGA

[16] G_SMBDAT — R485 4.7K_4 — Q43 2N7002 — MBDATA2 [8,13,32]

[15,16] +3V_VGA

U8250F

GND

Whistler Pro/Seymour XT_M2

PCIE_VSS#1	GND#1	A3
PCIE_VSS#2	GND#2	A37
PCIE_VSS#3	GND#3	AA16
PCIE_VSS#4	GND#4	AA18
PCIE_VSS#5	GND#5	AA2
PCIE_VSS#6	GND#6	AA21
PCIE_VSS#7	GND#7	AA23
PCIE_VSS#8	GND#8	AA26
PCIE_VSS#9	GND#9	AA28
PCIE_VSS#10	GND#10	AA6
PCIE_VSS#11	GND#11	AB12
PCIE_VSS#12	GND#12	AB15
PCIE_VSS#13	GND#13	AB17
PCIE_VSS#14	GND#14	AB20
PCIE_VSS#15	GND#15	AB22
PCIE_VSS#16	GND#16	AB24
PCIE_VSS#17	GND#17	AB27
PCIE_VSS#18	GND#18	AC11
PCIE_VSS#19	GND#19	AC13
PCIE_VSS#20	GND#20	AC16
PCIE_VSS#21	GND#21	AC18
PCIE_VSS#22	GND#22	AC2
PCIE_VSS#23	GND#23	AC21
PCIE_VSS#24	GND#24	AC23
PCIE_VSS#25	GND#25	AC26
PCIE_VSS#26	GND#26	AC28
PCIE_VSS#27	GND#27	AC6
PCIE_VSS#28	GND#28	AD15
PCIE_VSS#29	GND#29	AD17
PCIE_VSS#30	GND#30	AD20
PCIE_VSS#31	GND#31	AD22
PCIE_VSS#32	GND#32	AD24
PCIE_VSS#33	GND#33	AD27
PCIE_VSS#34	GND#34	AD9
PCIE_VSS#35	GND#35	AE2
	GND#36	AE6
	GND#37	AE10
	GND#38	AF16
	GND#39	AF18
	GND#40	AF21
	GND#41	AG17
GND#100	GND#42	AG2
GND#101	GND#43	AG20
GND#102	GND#44	AG22
GND#103	GND#45	AG6
GND#104	GND#46	AG9
GND#105	GND#47	AH21
GND#106	GND#48	A10
GND#107	GND#49	AJ11
GND#108	GND#50	AJ2
GND#109	GND#51	AJ28
GND#110	GND#52	AJ6
GND#111	GND#53	AK11
GND#112	GND#54	AK31
GND#113	GND#55	AK7
GND#114	GND#56	AL11
GND#115	GND#57	AL14
GND#116	GND#58	AL17
GND#117	GND#59	AL2
GND#118	GND#60	AL20
GND#119	GND/PX_EN#61	AL21 PX_EN_1
GND#120	GND#62	AL23
GND#121	GND#63	AL26
GND#122	GND#64	AL32
GND#123	GND#65	AL6
GND#124	GND#66	AL8
GND#125	GND#67	AM11
GND#126	GND#68	AM31
GND#127	GND#69	AM9
GND#128	GND#70	AN11
GND#129	GND#71	AN2
GND#130	GND#72	AN30
GND#131	GND#73	AN6
GND#132	GND#74	AN8
GND#133	GND#75	AP11
GND#134	GND#76	AP7
GND#135	GND#77	AP9
GND#136	GND#78	AR5
GND#137		
GND#138	GND#80	B11
GND#139	GND#81	B13
GND#140	GND#82	B15
GND#141	GND#83	B17
GND#142	GND#84	B19
GND#143	GND#85	B21
GND#144	GND#86	B23
GND#145	GND#87	B25
GND#146	GND#88	B27
GND#147	GND#89	B29
GND#148	GND#90	B31
GND#149	GND#91	B33
GND#150	GND#92	B7
GND#151	GND#93	B9
GND#153	GND#94	C1
GND#154	GND#95	C39
GND#155	GND#96	E35
GND#156	GND#97	E5
GND#157	GND#98	F11
GND#158	GND#99	F13
GND#159		
GND#160		
GND#161		
GND#163		
GND#164		
GND#165		
GND#166		
GND#167		
GND#168		
GND#169		
GND#170		
GND#171		
GND#172		
GND#173	VSS_MECH#1	A39
GND#174	VSS_MECH#2	AW1
GND#175	VSS_MECH#3	AW39
GND#152		
GND#162		

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMD Whistler (GD&Str)4/5	3A
Date: Wednesday, May 18, 2011	Sheet 17 of 47	

(VDDR1: 1.5V@9.1A)

(1.8V@500mA PCIE_VDDR)

(1.0V@2000mA PCIE_VDDC)

(1.8V@136mA VDD_CT)

(3.3V@60mA VDDR3)

VDDR4 for DVPDATA[12..23]

(VDDR4_5 : 1.8V@20/170mA)

VDDR5 for DVPDATA[0..11]

(1.8V@40mA PCIE_PVDD)

(SPV10 :1.0V@120mA)

(For MP7, 1.12V@4A VDDCI).

U8250E

POWER

Whistler Pro/Seymour XT_M2

	Rc	Rd
BACO Functions	NC	Stuff
NO BACO Functions	Stuff	NC

Rc

For non-BACO designs, connect BIF_VDDC to VDDC.
For BACO designs - see BACO reference schematics (ref138)

VGA Chip Pin N27,T27 don't use short pad ,use 0 ohm

Rd

BACO Functions Stuff

[42] VGACORESENSE

[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
[6,7,10,17,21,22,23,25,29,30,31,41] +5V
[14,16,17,43] +1.0V_VGA
[17,42] +VGACORE
[15,19,20,43] +1.5V_VGA
[14,16,43] +1.8V_VGA
[15,16] +3V_VGA

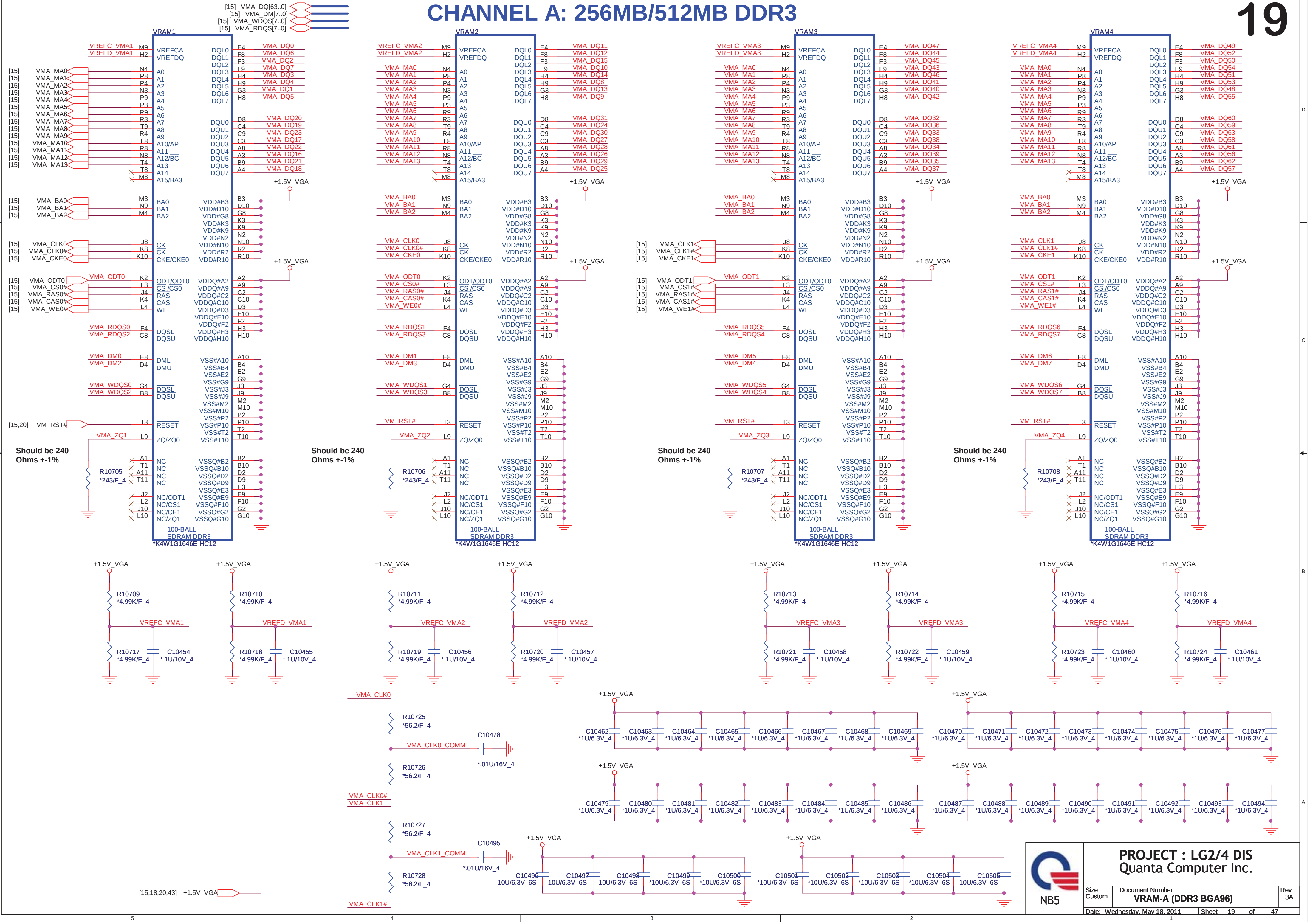
PROJECT : LG2/4 DIS
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	AMD Whistler (POWER) 5/5	3A

Date: Wednesday, May 18, 2011 Sheet 18 of 47

CHANNEL A: 256MB/512MB DDR3



PROJECT : LG2/4 DIS
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	VRAM-A (DDR3 BGA96)	3A

Date: Wednesday, May 18, 2011 Sheet 19 of 47

CHANNEL B: 256MB/512MB DDR3

[15] VMB_DQ[63..0]
[15] VMB_DM[7..0]
[15] VMB_WDQS[7..0]
[15] VMB_RDQS[7..0]

VRAM5 / VRAM6 / VRAM7 / VRAM8

K4W1G1646E-HC12

100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R10729 243/F_4
R10730 243/F_4
R10731 243/F_4
R10732 243/F_4

+1.5V_VGA

R10733 4.99K/F_4
R10734 4.99K/F_4
R10735 4.99K/F_4
R10736 4.99K/F_4
R10737 4.99K/F_4
R10738 4.99K/F_4
R10739 4.99K/F_4
R10740 4.99K/F_4

VREFC_VMB1 / VREFD_VMB1
VREFC_VMB2 / VREFD_VMB2
VREFC_VMB3 / VREFD_VMB3
VREFC_VMB4 / VREFD_VMB4

R10741 4.99K/F_4 C10506 .1U/10V_4
R10742 4.99K/F_4 C10507 .1U/10V_4
R10743 4.99K/F_4 C10508 .1U/10V_4
R10744 4.99K/F_4 C10509 .1U/10V_4
R10745 4.99K/F_4 C10510 .1U/10V_4
R10746 4.99K/F_4 C10511 .1U/10V_4
R10747 4.99K/F_4 C10512 .1U/10V_4
R10748 4.99K/F_4 C10513 .1U/10V_4

VMB_CLK0
VMB_CLK0_COMM
VMB_CLK0#
VMB_CLK1
VMB_CLK1_COMM
VMB_CLK1#

R10749 56.2/F_4
R10750 56.2/F_4
R10751 56.2/F_4
R10752 56.2/F_4

C10530 .01U/16V_4
C10547 .01U/16V_4

C10520 C10521 C10522 C10523 C10524 C10525 C10527 C10528 1U/6.3V_4
C10531 C10532 C10533 C10534 C10535 C10536 C10537 C10538 1U/6.3V_4
C10514 C10515 C10516 C10517 C10518 C10519 C10526 C10529 1U/6.3V_4
C10539 C10540 C10541 C10542 C10543 C10544 C10545 C10546 1U/6.3V_4
C10548 C10549 C10550 C10551 C10552 C10553 C10554 C10555 C10556 C10557 10U/6.3V_6S

[15,18,19,43] +1.5V_VGA

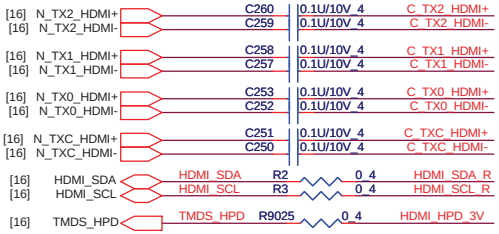
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-B (DDR3 BGA96)	3A

Date: Thursday, May 19, 2011 Sheet 20 of 47

For DIS HDMI Only



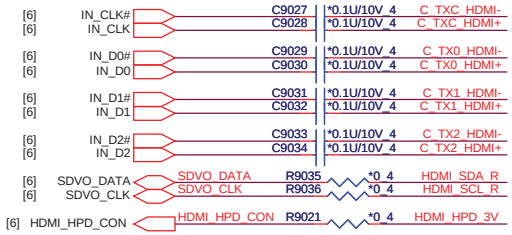
	Select
Dis	Ra
muxless	Rb

Ra

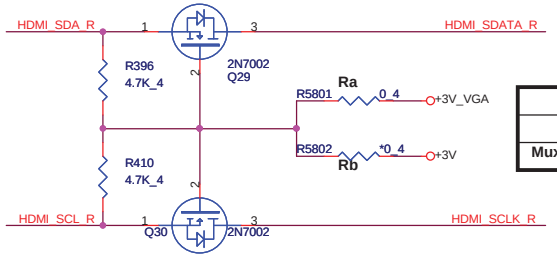
	Select
Dis	Ra
Muxless	Rb

Rb

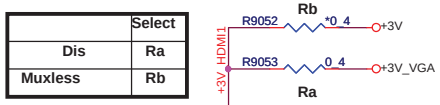
For Muxless/UMA HDMI function

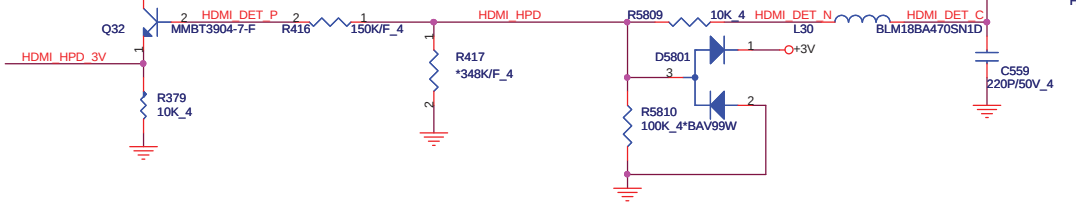


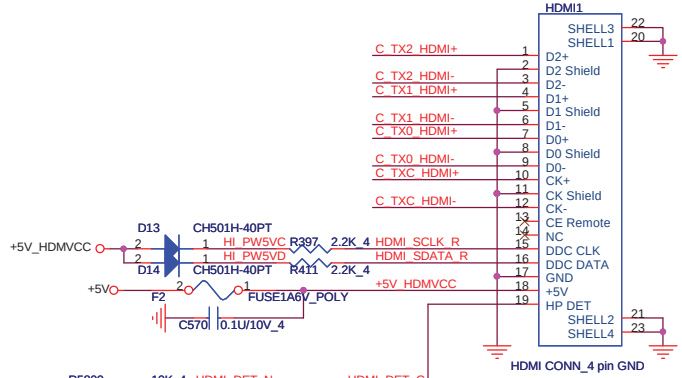
DIS: 4.7K
UMA/Muxless: 2.2K

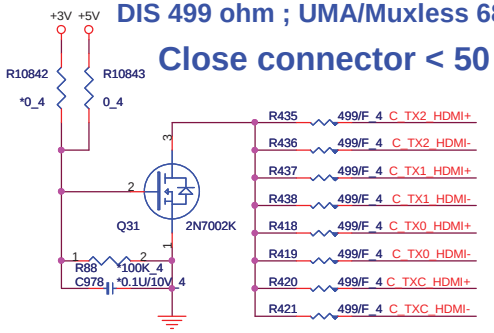


	Select
Dis	Ra
Muxless	Rb









DIS 499 ohm ; UMA/Muxless 680 ohm

Close connector < 50 mil

Close connector < 50 mil

EMI

C_TXC_HDMI+	R135	150/F_4	C_TXC_HDMI-
C_TX0_HDMI+	R136	150/F_4	C_TX0_HDMI-
C_TX1_HDMI+	R141	150/F_4	C_TX1_HDMI-
C_TX2_HDMI+	R142	150/F_4	C_TX2_HDMI-

DV2 Change to 150 ohm

+5VCRT

[6,7,10,17,22,23,25,29,30,31,41] +5V
[2,6,7,8,9,10,12,13,14,17,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI and connector	3A

Date: Friday, May 20, 2011 Sheet 21 of 47

	Select
Dis	Ra
muxless	Rb

Rb MUXLESS

[6] PCH_LA_CLK	PCH_LA_CLK	R54	*0_4	TXLCLKOUT+	
[6] PCH_LA_CLK#	PCH_LA_CLK#	R55	*0_4	TXLCLKOUT-	
[6] PCH_LA_DATAP0	PCH_LA_DATAP0	R57	*0_4	TXLOUT0+	
[6] PCH_LA_DATAN0	PCH_LA_DATAN0	R56	*0_4	TXLOUT0-	
[6] PCH_LA_DATAP1	PCH_LA_DATAP1	R41	*0_4	TXLOUT1+	
[6] PCH_LA_DATAN1	PCH_LA_DATAN1	R40	*0_4	TXLOUT1-	
[6] PCH_LA_DATAP2	PCH_LA_DATAP2	R38	*0_4	TXLOUT2+	
[6] PCH_LA_DATAN2	PCH_LA_DATAN2	R39	*0_4	TXLOUT2-	
[6] PCH_LB_CLK	PCH_LB_CLK	R50	*0_4	TXUCLKOUT+	
[6] PCH_LB_CLK#	PCH_LB_CLK#	R51	*0_4	TXUCLKOUT-	
[6] PCH_LB_DATAP0	PCH_LB_DATAP0	R36	*0_4	TXUOUT0+	
[6] PCH_LB_DATAN0	PCH_LB_DATAN0	R37	*0_4	TXUOUT0-	
[6] PCH_LB_DATAP1	PCH_LB_DATAP1	R52	*0_4	TXUOUT1+	
[6] PCH_LB_DATAN1	PCH_LB_DATAN1	R53	*0_4	TXUOUT1-	
[6] PCH_LB_DATAP2	PCH_LB_DATAP2	R34	*0_4	TXUOUT2+	
[6] PCH_LB_DATAN2	PCH_LB_DATAN2	R35	*0_4	TXUOUT2-	

Ra DIS

[16] GPU_TXLCLKOUT+	GPU_TXLCLKOUT+	R46	0_4	TXLCLKOUT+
[16] GPU_TXLCLKOUT-	GPU_TXLCLKOUT-	R47	0_4	TXLCLKOUT-
[16] GPU_TXLOUT0+	GPU_TXLOUT0+	R49	0_4	TXLOUT0+
[16] GPU_TXLOUT0-	GPU_TXLOUT0-	R48	0_4	TXLOUT0-
[16] GPU_TXLOUT1+	GPU_TXLOUT1+	R32	0_4	TXLOUT1+
[16] GPU_TXLOUT1-	GPU_TXLOUT1-	R31	0_4	TXLOUT1-
[16] GPU_TXLOUT2+	GPU_TXLOUT2+	R29	0_4	TXLOUT2+
[16] GPU_TXLOUT2-	GPU_TXLOUT2-	R30	0_4	TXLOUT2-
[16] GPU_TXUCLKOUT+	GPU_TXUCLKOUT+	R42	0_4	TXUCLKOUT+
[16] GPU_TXUCLKOUT-	GPU_TXUCLKOUT-	R43	0_4	TXUCLKOUT-
[16] GPU_TXUOUT0+	GPU_TXUOUT0+	R27	0_4	TXUOUT0+
[16] GPU_TXUOUT0-	GPU_TXUOUT0-	R28	0_4	TXUOUT0-
[16] GPU_TXUOUT1+	GPU_TXUOUT1+	R44	0_4	TXUOUT1+
[16] GPU_TXUOUT1-	GPU_TXUOUT1-	R45	0_4	TXUOUT1-
[16] GPU_TXUOUT2+	GPU_TXUOUT2+	R25	0_4	TXUOUT2+
[16] GPU_TXUOUT2-	GPU_TXUOUT2-	R26	0_4	TXUOUT2-

Rb MUXLESS

[6] PCH_LVDS_BLON	R298	*0_4	LVDS_BLON
[6] PCH_DISP_ON	R323	*0_4	DISP_ON
[6] PCH_DPST_PWM	R305	*0_4	DPST_PWM

Ra DIS

[16,17] GPU_LVDS_BLON	R297	0_4	LVDS_BLON
[16] GPU_DISP_ON	R324	0_4	DISP_ON
[16] GPU_DPST_PWM	R303	0_4	DPST_PWM

Rb MUXLESS

+3V

	R13	*2.2K_4	PCH_EDIDCLK
	R14	*2.2K_4	PCH_EDIDDATA
[6] PCH_EDIDCLK	PCH_EDIDCLK	R11	*0_4 EDIDCLK
[6] PCH_EDIDDATA	PCH_EDIDDATA	R12	*0_4 EDIDDATA

Ra DIS

[16] GPU_EDIDCLK	GPU_EDIDCLK	R8	0_4 EDIDCLK
[16] GPU_EDIDDATA	GPU_EDIDDATA	R9	0_4 EDIDDATA

+VIN_BLIGHT

+VIN — L1 UPB201209T-330Y-N — +VIN_BLIGHT

C2 *.1U/50V_6 — C441 .1U/50V_6 — C6 .01U/25V_4 — C4 .1U/50V_6

EDIDCLK C13 *10P/50V_4
EDIDDATA C14 *10P/50V_4

DIGITAL_D1 C11 10P/50V_4
DIGITAL_CLK_L C8 10P/50V_4
for EMI issue

R300 100K/F_4
C444 22P/50V_4

[32] LID_CONTROL — R9079 *0_4/S_PN_BLON — D8 RB501V-40 — BLON_CON

LVDS_BLON R294 1K/F_4 — D7 *RB501V-40 — LID_EC# [31,32]
R295 100K/F_4 — R299 47K_4 — +3VPCU

[8] LCD_BK — Q20 *DTC144EUA

+3V — C453 1000P/50V_4

LVDS1 — +3VLCD_CON

EDIDCLK
EDIDDATA
TXLOUT0-
TXLOUT0+
TXLOUT1-
TXLOUT1+
TXLOUT2-
TXLOUT2+
TXLCLKOUT-
TXLCLKOUT+
TXUOUT0-
TXUOUT0+
TXUOUT1-
TXUOUT1+
TXUOUT2-
TXUOUT2+
TXUCLKOUT-
TXUCLKOUT+

GS12401-1011-9F

L2 SBK160808T-601Y-N
[25] DIGITAL_D1 — L3 SBK160808T-601Y-N — DIGITAL_D1_CN
[25] DIGITAL_CLK — DIGITAL_CLK_L
+5V_CAM
[8] USBP9- — L22 WCM2012-90 — USBP9- L
[8] USBP9+ — USBP9+ L
Webcam
DPST_PWM
BLON_CON
+VIN_BLIGHT
C445 22P/50V_4

+3V — C10763 1U/6.3V_4 — U8254 IC(5P) G5243AT11U — +LCDVCC
DISP_ON — R10885 100K/F_4
IN — OUT — L8041 HCB2012KF-600T30/3A_8
IN — GND
ON/OFF

C10764 *0.01U/25V_4 — C10765 0.1U/10V_4 — C10766 10U/6.3V_8

+3VLCD_CON

+5V — L28 HCB2012KF-600T30 — +5V_CAM
C447 0.01U/16V_4
C449 10U/6.3V_8

+3VPCU — C443 0.1U/10V_4

U8253

[7,29,32] LAD0 — LAD0
[7,29,32] LAD1 — LAD1
[7,29,32] LAD2 — LAD2
[7,29,32] LAD3 — LAD3
[8] CLK_PCI_TPM — CLK_PCI_TPM
LCLK

[7,29,32] LFRAME# — LFRAME#
[2,8,14,24,27,28,29,32] PLTRST# — PLTRST#
LPCPD#_TPM
[7,32] SERIRQ — SERIRQ

[6,32] CLKRUN# — CLKRUN#

TEST/BADD
NC
NC
NC

VDD
VDD
VDD
VSB
GND
GND
GND
GND
GPIO
GPIO2
PP
TESTI
XTALI/32K IN
XTALO

SLB9635

C10756 C10757 C10758 C10759 0.1U

R10874 *4.7K — R10875 *4.7K
R10879 *4.7K — R10880 *4.7K

R10877 *0
R10878 0/4

TPM_XIN — TPM_XOUT — 32.768KHZ — Y8024
C10761 18P — C10762 18P

+3V — R450 4.7K/F_4 — LPCPD#_TPM

+3V — R10881 4.7K — R10882 *4.7K

[6,32] SLP_S5 — R10883 *0
[6] SUS_STAT# — R10884 *0 — LPCPD#_TPM

TPM (1.2)

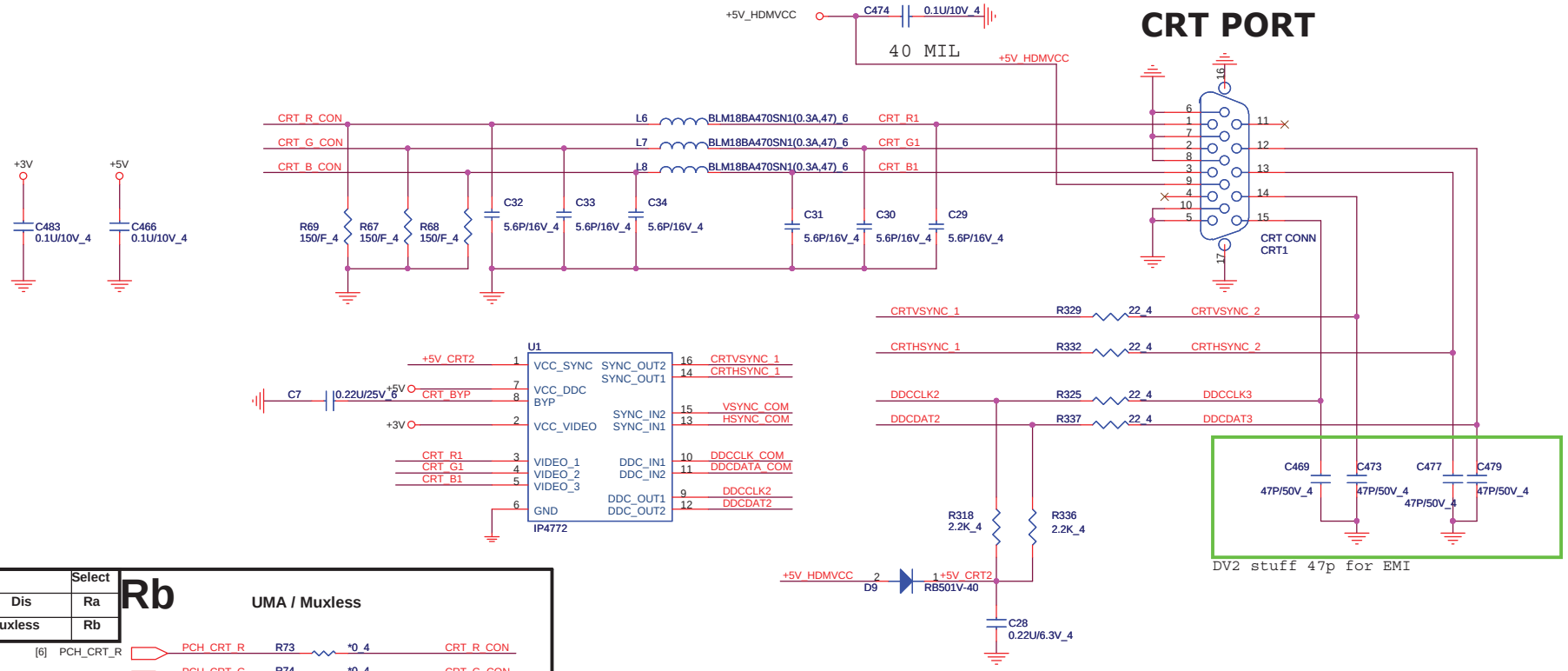
[2,6,7,8,9,10,12,13,14,17,21,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
[10,28,29,31,34,35,36,37,38,39,40,41,42,43] +5VS5
[6,7,10,17,21,23,25,29,30,31,41] +5V
[26,29,33,34,35,36,37,40,41,42,43] +VIN
[7,31,32,33,34] +3VPCU
[30,41,43] +12VALW

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID function	3A
Date: Thursday, May 19, 2011	Sheet 22 of 47	

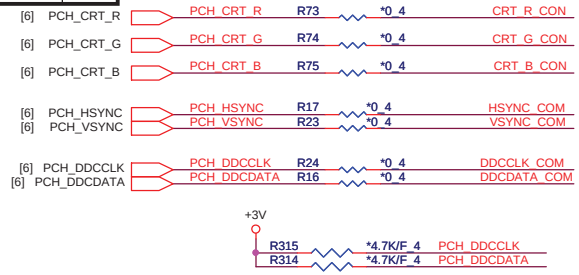
CRT PORT



	Select
Dis	Ra
muxless	Rb

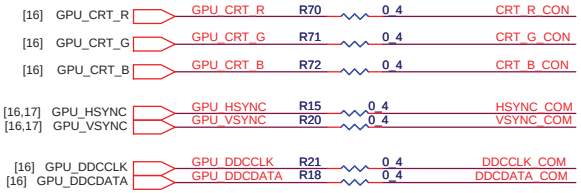
Rb

UMA / Muxless



Ra

DIS Only



DIS Only / Muxless stuff

+5VCRT

[6,7,10,17,21,22,25,29,30,31,41] +5V

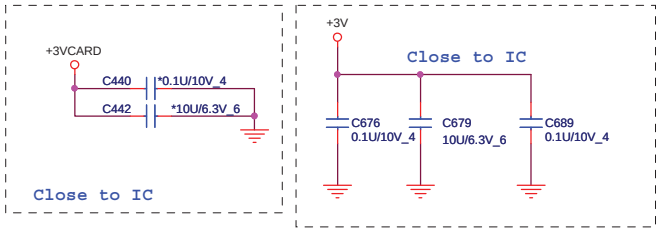
[2,6,7,8,9,10,12,13,14,17,21,22,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V

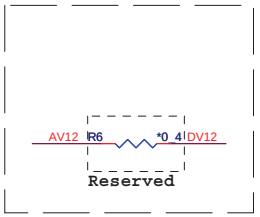
NB5

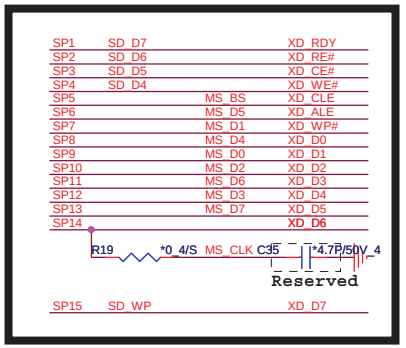
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	3A

Date: Wednesday, May 18, 2011 Sheet 23 of 47

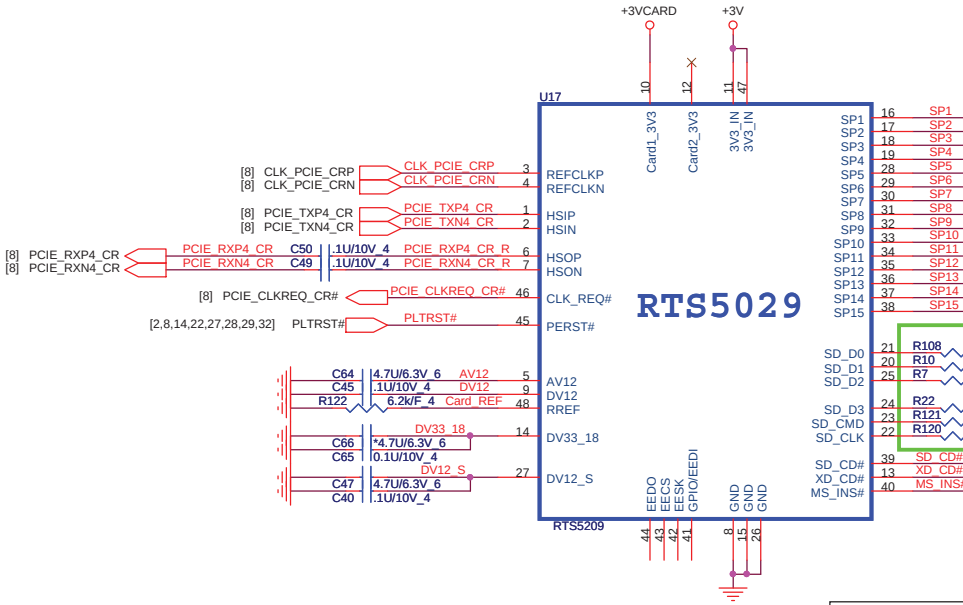


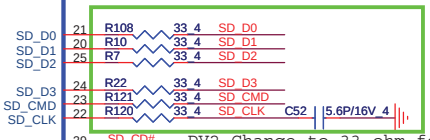


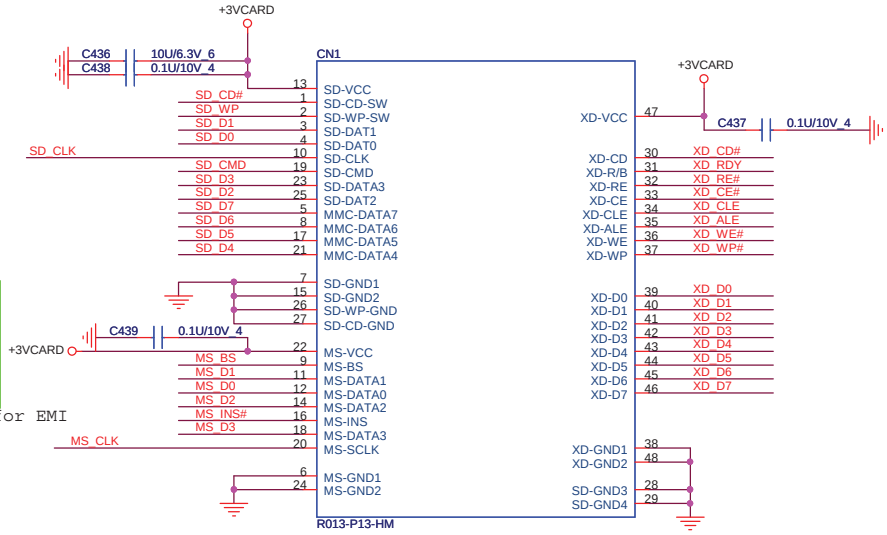


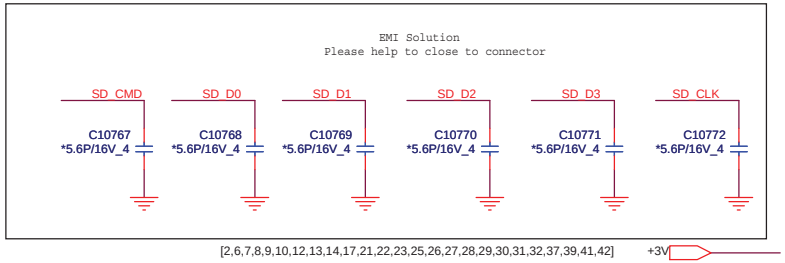
Share Pin

7-in-1 flash media slot(SD / SDHC / SDXC(UHS 104) / MS/MMC/ XD/ MSP)





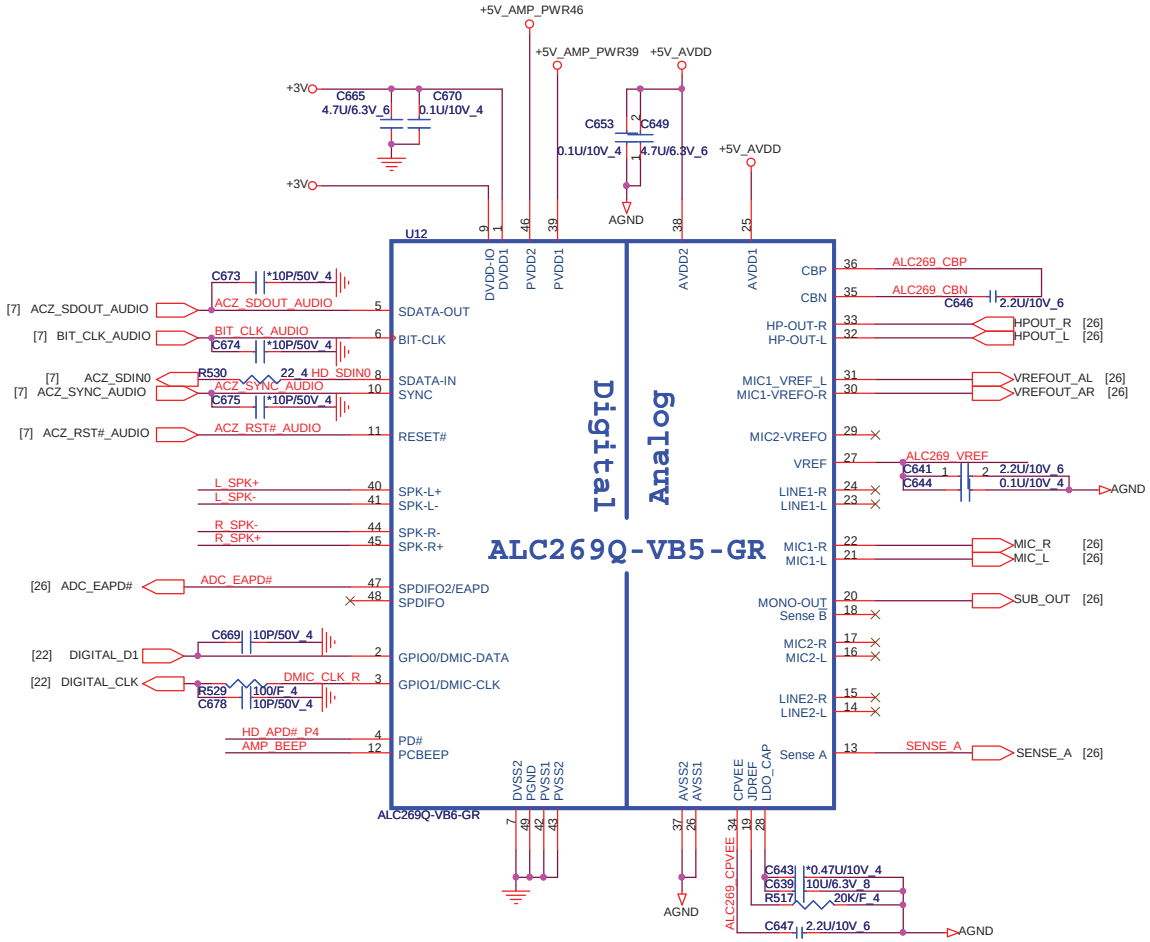


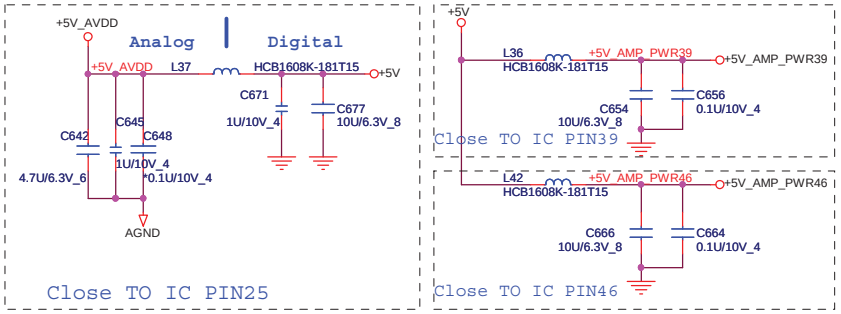


NB5

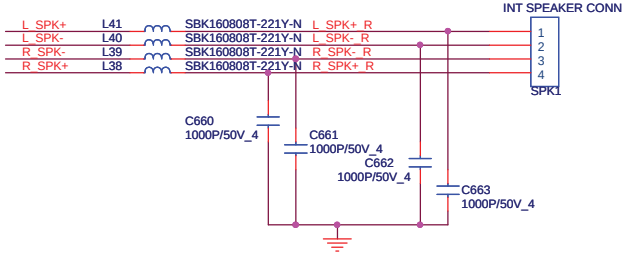
PROJECT : LG2/4 DIS
Quanta Computer Inc.

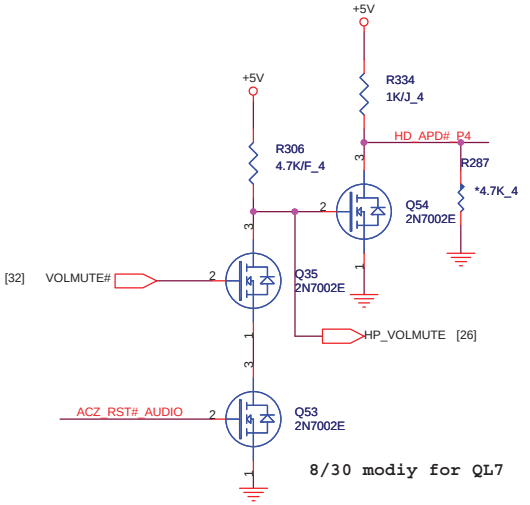
Size	Document Number	Rev
Custom	Card reder (RTS5029)	3A
Date: Wednesday, May 18, 2011	Sheet 24 of 47	



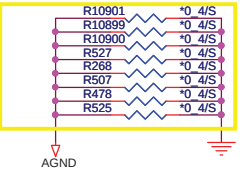


INT. SPEAKER





PV
Change to Shortpad



NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDA Azalia ALC269	3A

Date: Thursday, May 19, 2011 Sheet 25 of 47

Line out

Normal Open Jack

HPO1

HP-JACK-BLACK

AGND SHIELD

[25] HPOUT_L → HPOUT_L → R504 75_4 → HPOUT_L1 → L35 SBK160808T-301Y-N → HPOUT_L2

[25] HPOUT_R → HPOUT_R → R500 75_4 → HPOUT_R1 → L34 SBK160808T-301Y-N → HPOUT_R2

+3V

R508 *220K_4

Q47 *ME2303T1

[25] ADC_EAPD#

[25] HP_VOLMUTE

R514 *0_4 R515 *4.7K_4

R516 *4.7K_4 C504 *1U/10V_4

R512 *0_4 R513 *0_4

Q49 *AP2302GN

Q51 *AP2302GN

R510 *1K/F_4

R511 *1K/F_4

C640 150P/50V_4 C637 150P/50V_4

C638 *150P/50V_4 C634 *150P/50V_4

AGND

SENSE_PHONE R506 39.2K/F_4 SENSE_A SENSE_A [25]

Reduce headphone POP

HPOUT_L2 HPOUT_R2

CD3 CD4 Clamp-Diode Clamp-Diode

MIC_IN_R MIC_IN_L

CD2 CD1 Clamp-Diode Clamp-Diode

MIC

Normal Open Jack

MIC1 HP-JACK-BLACK

[25] VREFOUT_AR → VREFOUT_AR

[25] VREFOUT_AL → VREFOUT_AL

R258 4.7K/F_4 R229 4.7K/F_4 C348 *1U/10V_4

C406 *1U/10V_4

C361 100P/50V_4

C389 4.7U/6.3V_6

[25] MIC_L → MIC_L → MIC_L1_RC → R252 1K/F_4 → MIC_L1 → L24 SBK160808T-301Y-N → MIC_IN_L

[25] MIC_R → MIC_R → C354 4.7U/6.3V_6 → MIC_R1_RC → R228 1K/F_4 → MIC_R1 → L23 SBK160808T-301Y-N → MIC_IN_R

C337 100P/50V_4

SENSE_A 20K/F_4 R505 SENSE_MIC

SENSE_PHONE SENSE_MIC

CD5 CD6 Clamp-Diode Clamp-Diode

Sub-Woofer for 17"

+VIN PVCC2

R10849 *0_8/S short0805

PV change to short pad

U8252 *HPA00836

Pin		Pin	
1	SD	28	PVCCL
2	FAULT	27	PVCCL
3	NC_3	26	BSN_26
4	NC_4	25	OUTN_25
5	GAIN0	24	PGND
6	GAIN1	23	OUTN_23
7	AVCC	22	BSN_22
8	AGND	21	BSP_21
9	GVDD	20	OUTP_20
10	PLIMIT	19	PGND
11	INN	18	OUTP_18
12	INP	17	BSP_17
13	NC_13	16	PVCC
14	AVCC	15	PVCC
29	GND		

+3V R10845 *100K_4 → ADC_EAPD# ← [25] ADC_EAPD#

+3V R10848 *100K_4

PVCC2 R10850 *100K_6

R10852 *100K_6

SUB_GND R10851 *0_6/S

R10854 *0_6/S

PVCC2 R10856 *10_6 C10735 *1U/25V_6

SUB_GND C10737 *1U/25V_6

R10858 *47.5K/F_6

SUB_GND C10738 *1U/25V_6 R10859 *27.4K/F_6

SUB_GND C10741 *1U/25V_6 R8034 *0_6

[25] SUB_OUT SUB_OUT C10742 *1U/25V_6 R8036 *0_6

PVCC2 R10860 *10K_6

C10730 *1000P/50V_6 C10731 *0.1U/50V_6 C10732 *100U/25V L-F

C10733 *0.22U/50V_8

C10734 *0.22U/50V_8

C10736 *0.22U/50V_8

C10743 *0.22U/50V_8

C10744 *1000P/50V_6 C10745 *0.1U/50V_6

SUB_GND PVCC2

L8037 *PBY160808T-151Y-N SUB_OUT+

L8038 *PBY160808T-151Y-N SUB_OUT-

CN8202 *88266-020L

C10739 *1000P/50V_4 C10740 *1000P/50V_4

R10844 *0_4 L8036 *0_8 R10846 *0_6 R10847 *0_4

R10853 *0_8 R10855 *0_8

R10857 *0_8

GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

[22,29,33,34,35,36,37,40,41,42,43] +VIN

[6,7,10,17,21,22,23,25,29,30,31,41] +5V

[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,27,28,29,30,31,32,37,39,41,42] +3V

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Audio Jack/Accelerometer	3A

Date: Wednesday, May 18, 2011 Sheet 26 of 47

Atheros Lan

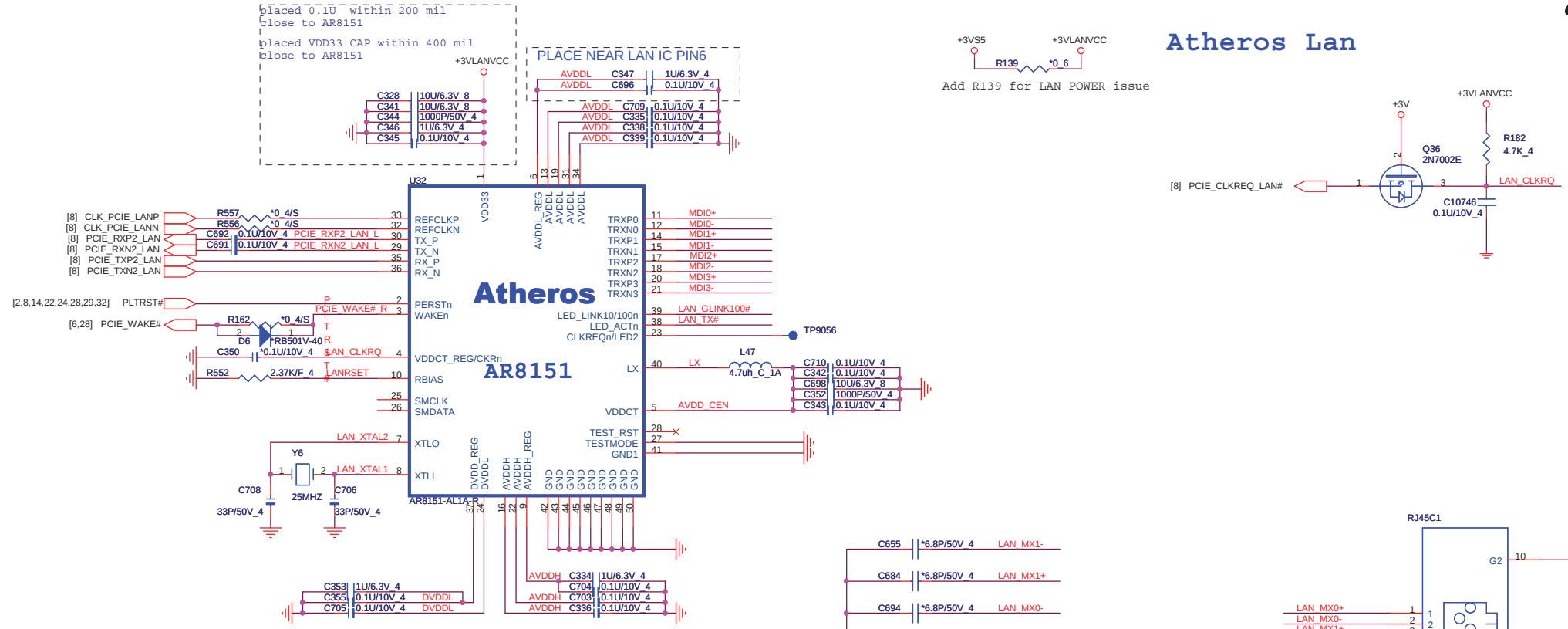
placed 0.1U within 200 mil close to AR8151

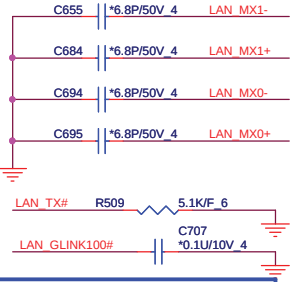
placed VDD33 CAP within 400 mil close to AR8151

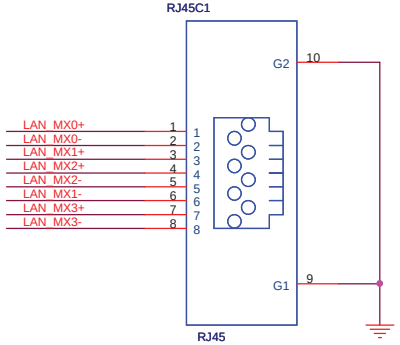
PLACE NEAR LAN IC PIN6

+3VS5 — R139 *0_6 — +3VLANVCC

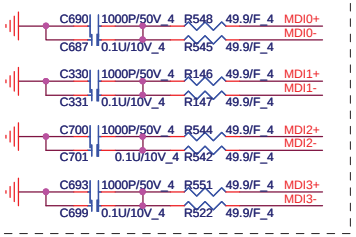
Add R139 for LAN POWER issue



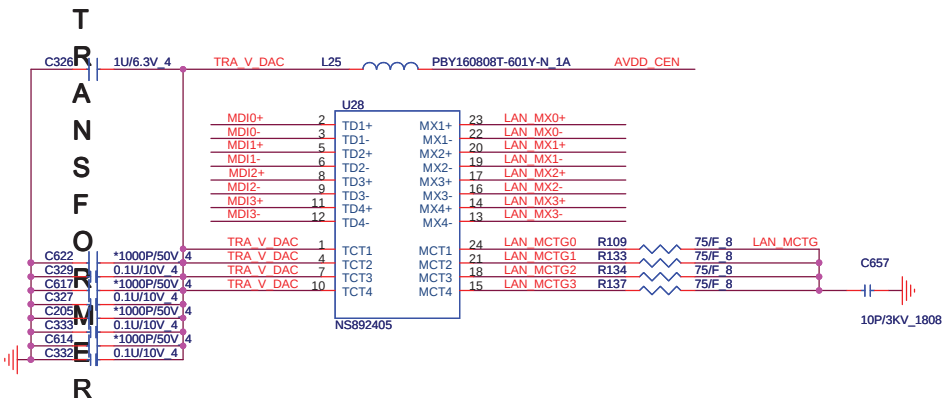




PLACE NEAR LAN IC SIDE



TRANSFORMER



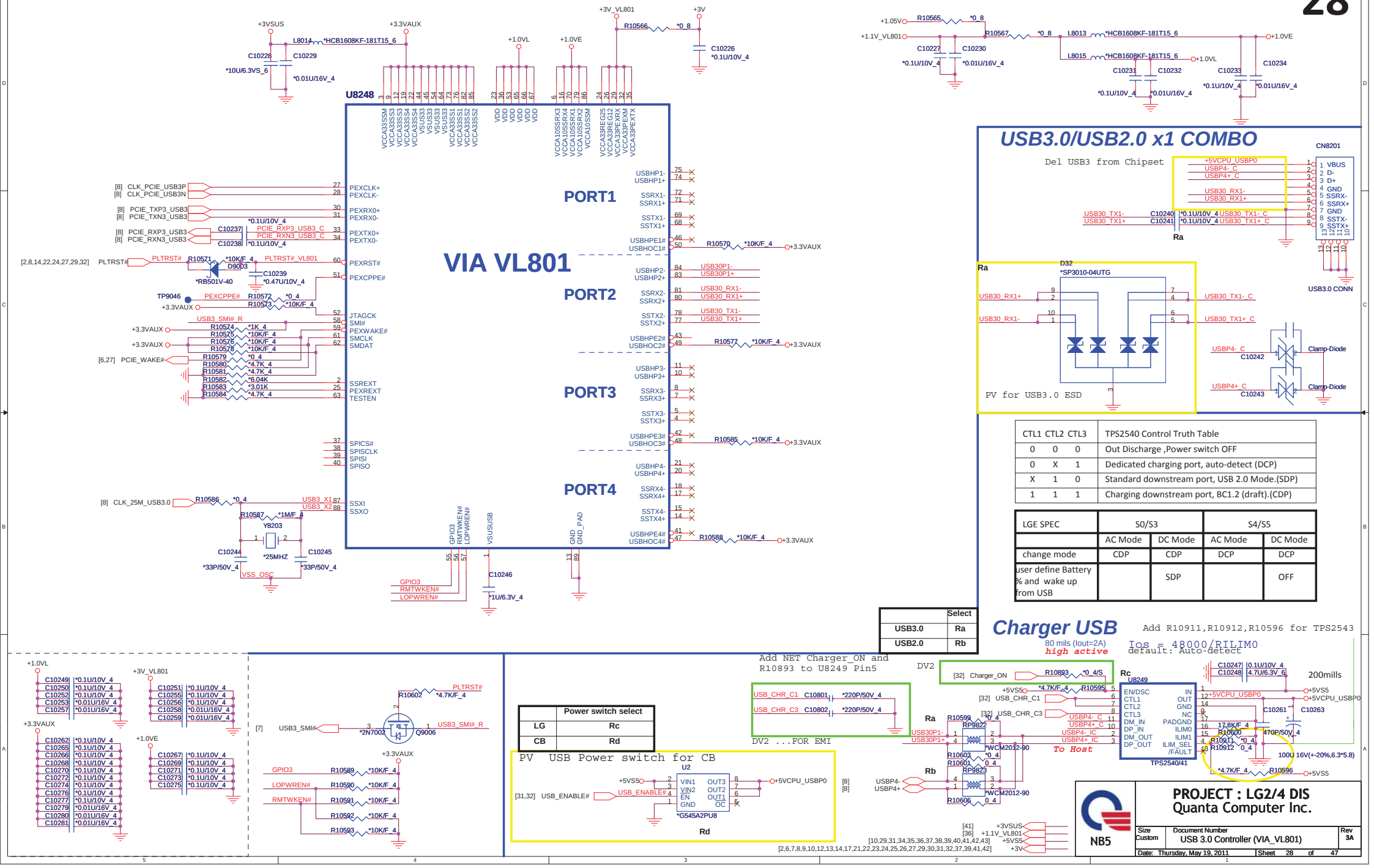
[2,6,7,8,9,10,29,32,34,37,38,41,43] +3VS5
[41] +3VLANVCC
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,39,41,42] +3V

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN AR8151/RJ45	3A

Date: Wednesday, May 18, 2011 Sheet 27 of 47



CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated charging port, auto-detect (DCP)
X	1	0	Standard downstream port, USB 2.0 Mode.(SDP)
1	1	1	Charging downstream port, BC1.2 (draft).(CDP)

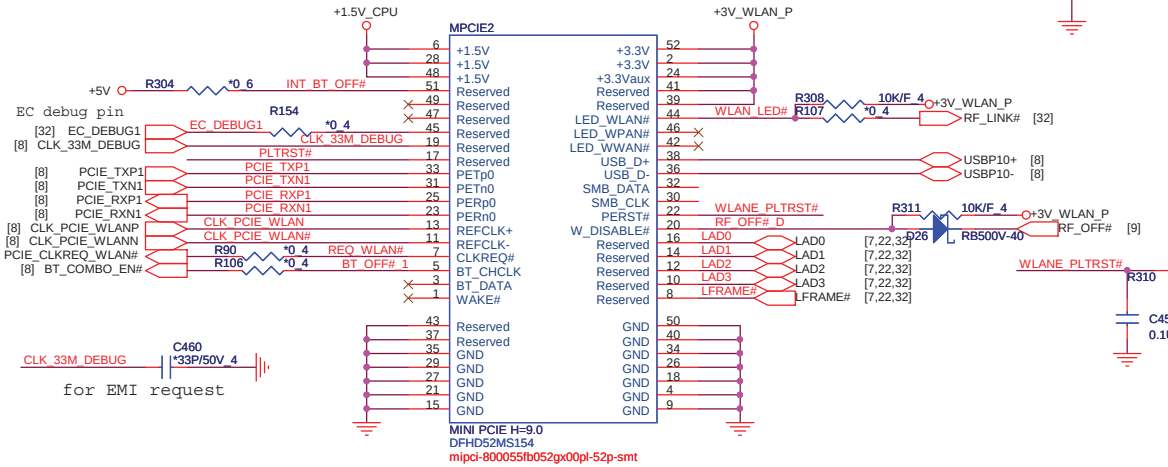
LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
change mode	CDP	CDP	DCP	DCP
user define Battery % and wake up from USB		SDP		OFF

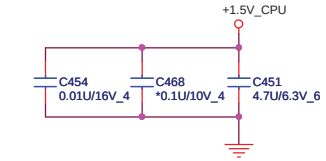
	Select
USB3.0	Ra
USB2.0	Rb

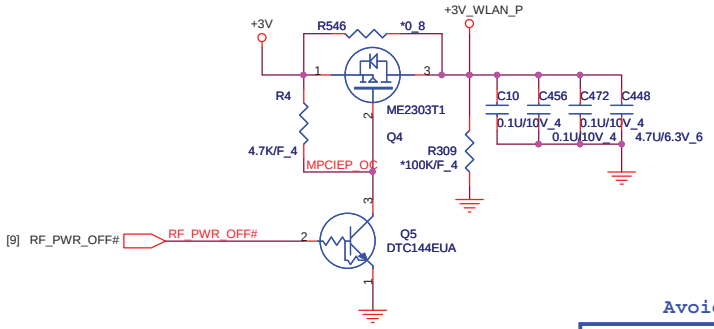
	Power switch select
LG	Rc
CB	Rd

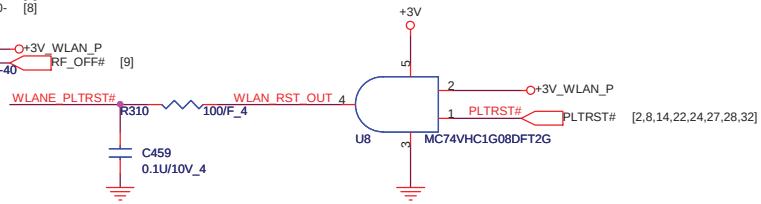
Size	Document Number
Custom	USB 3.0 Controller (VIA_VL801)
Date: Thursday, May 19, 2011	Sheet 28 of 47

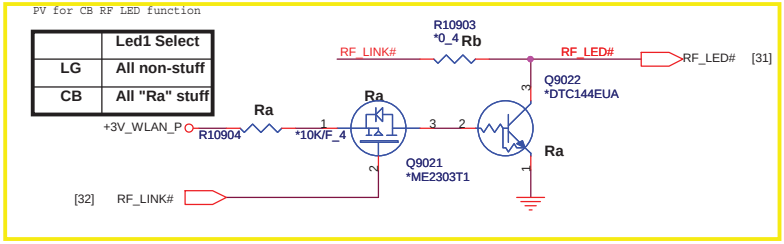
Mini PCI-E Card 1 - Half WLAN

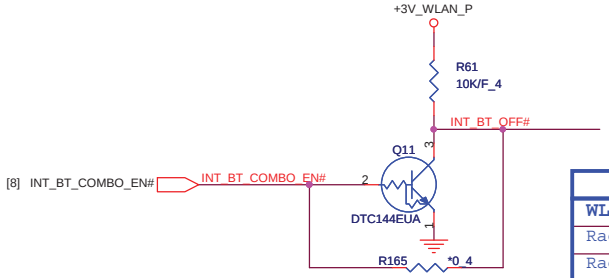








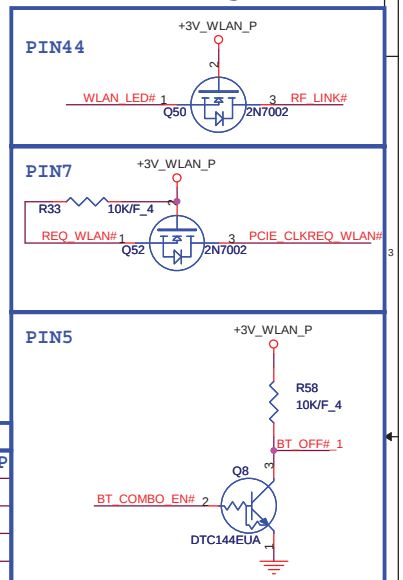




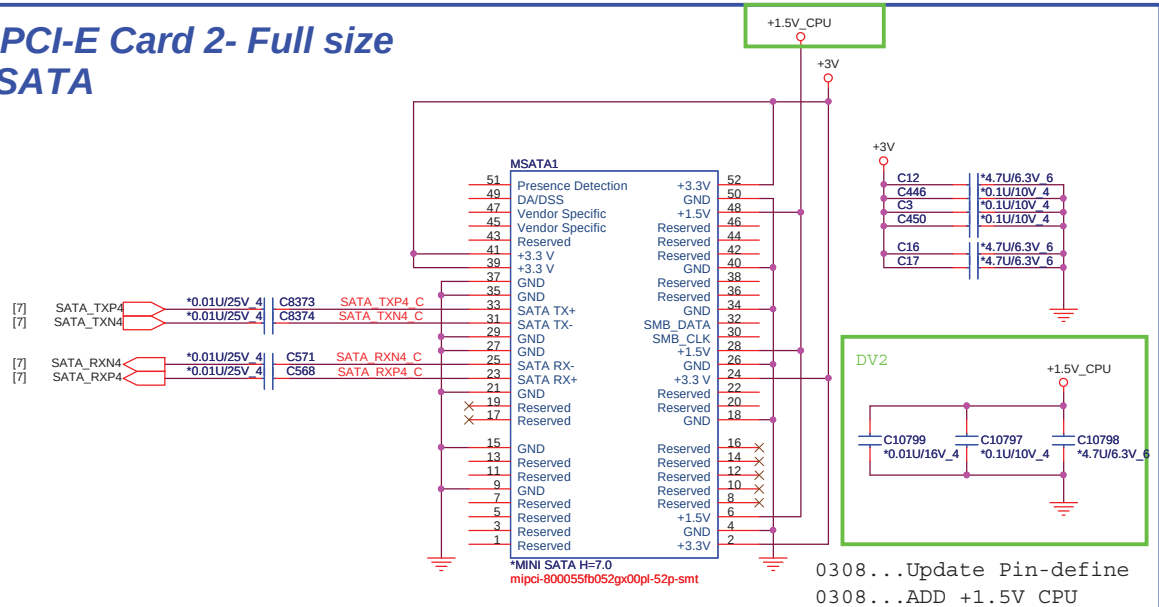
LGE mini-pcie power status

WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	**Radio-OFF**	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	**Radio-OFF**	**Power-OFF**

Avoid leakage issue

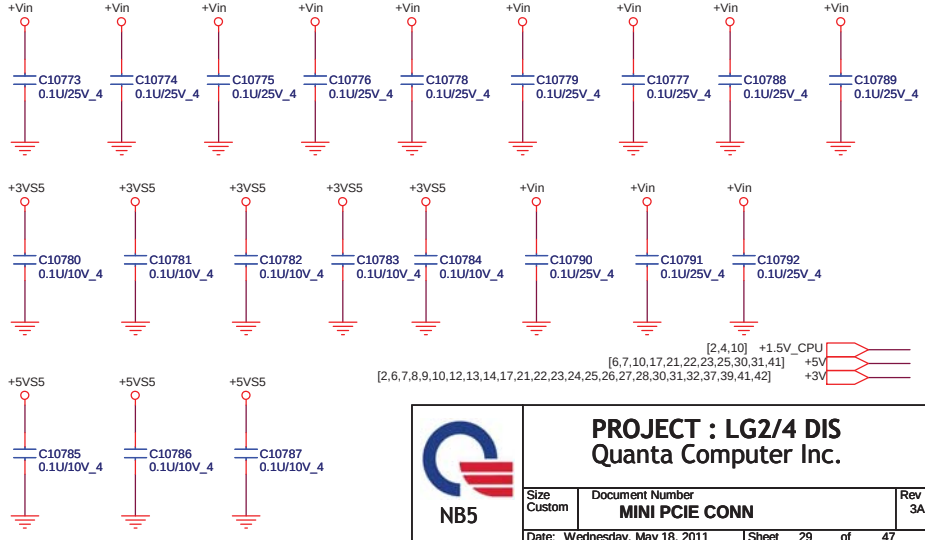


Mini PCI-E Card 2- Full size MINISATA



0308...Update Pin-define
0308...ADD +1.5V_CPU

Power Plan Cap for EMI



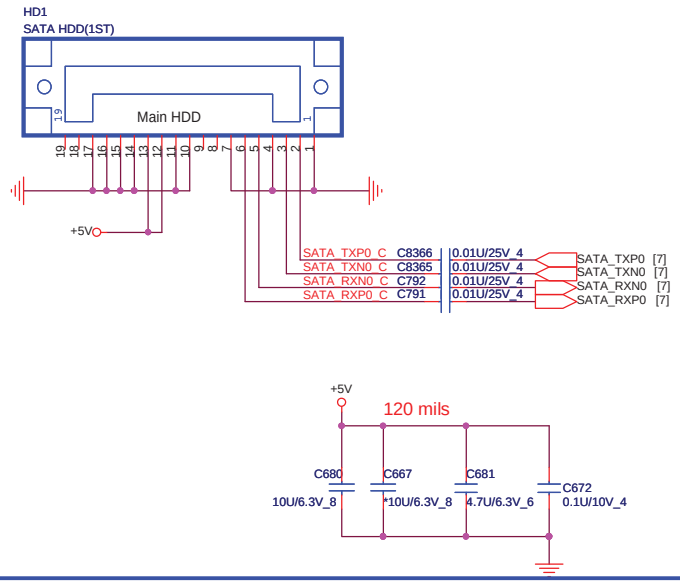
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN	3A
Date: Wednesday, May 18, 2011	Sheet 29 of 47	

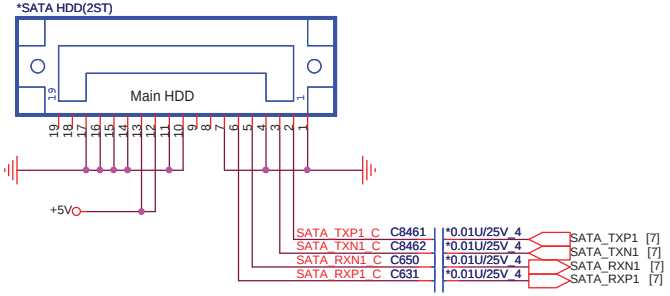
MAIN SATA HDD

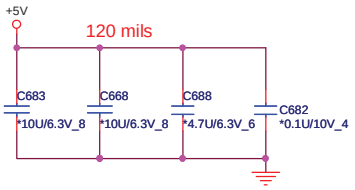
DC Current rating: 0.5 A



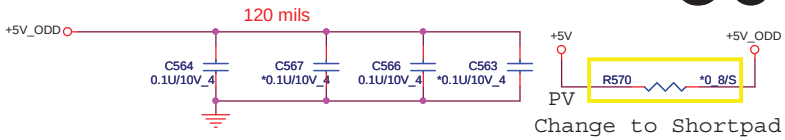
2nd SATA HDD for 17"

DC Current rating: 0.5 A



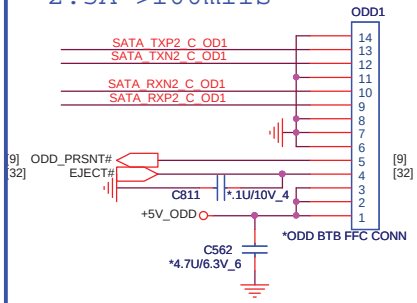


SATA CD-ROM To ODD Board



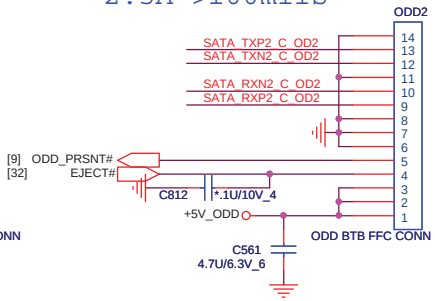
For 17" place

2.5A >100mils



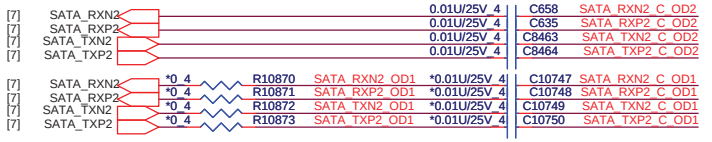
For 14"/15" place

2.5A >100mils



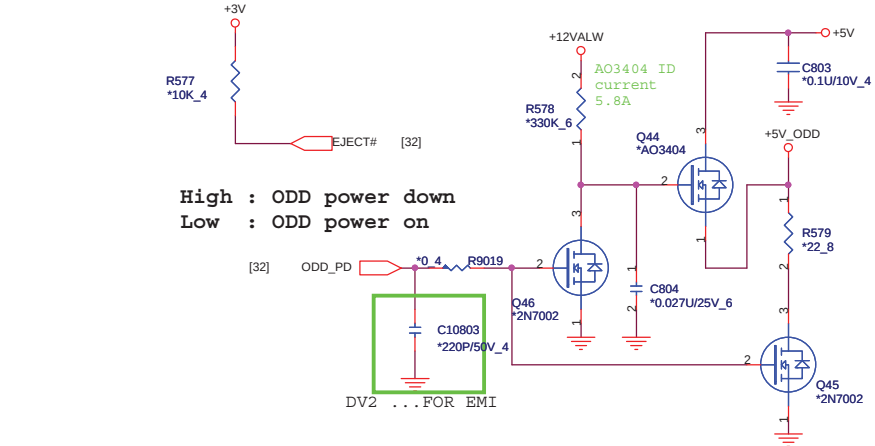
Ra FOR 14"/15"
Rb FOR 17"

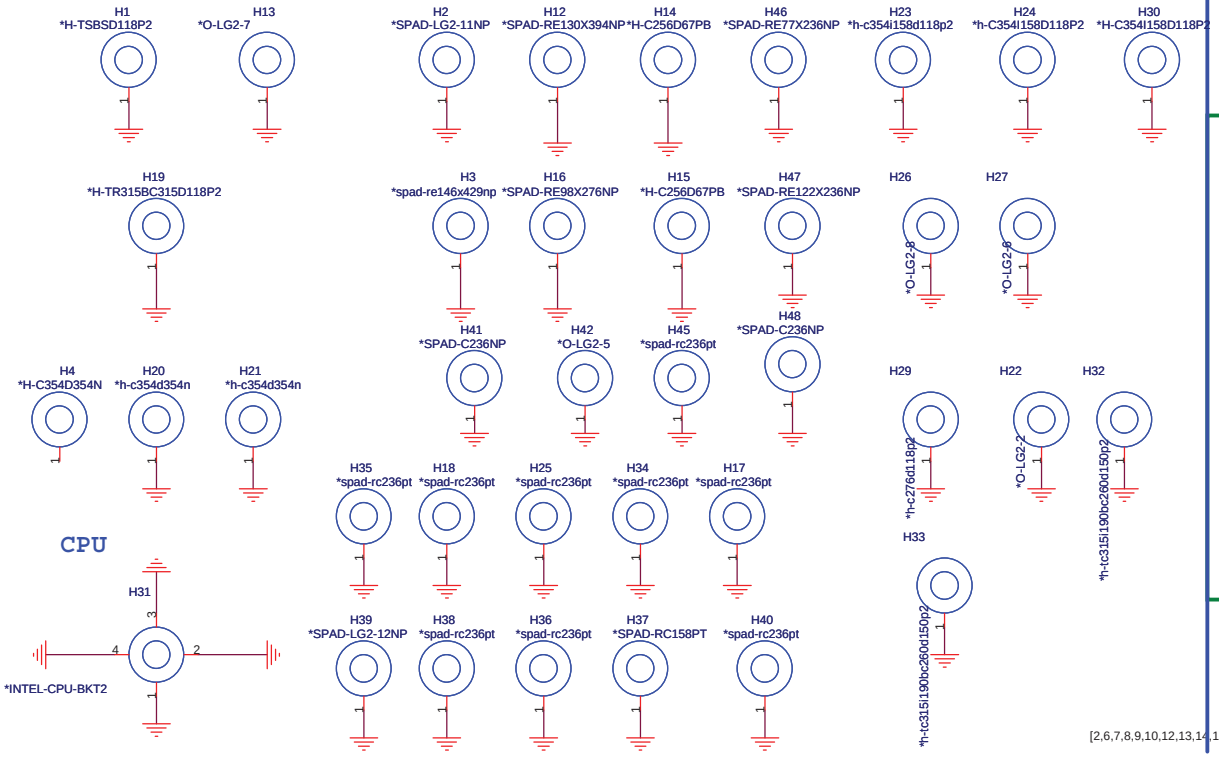
Ra



Rb

Rb





[41,43] +12VALW
[6,7,10,17,21,22,23,25,29,31,41] +5V
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,31,32,37,39,41,42] +3V

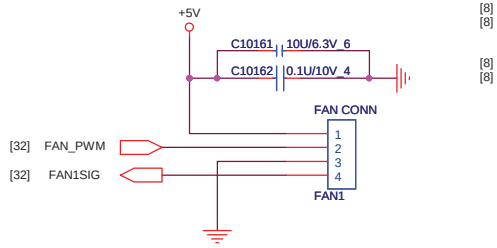
NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

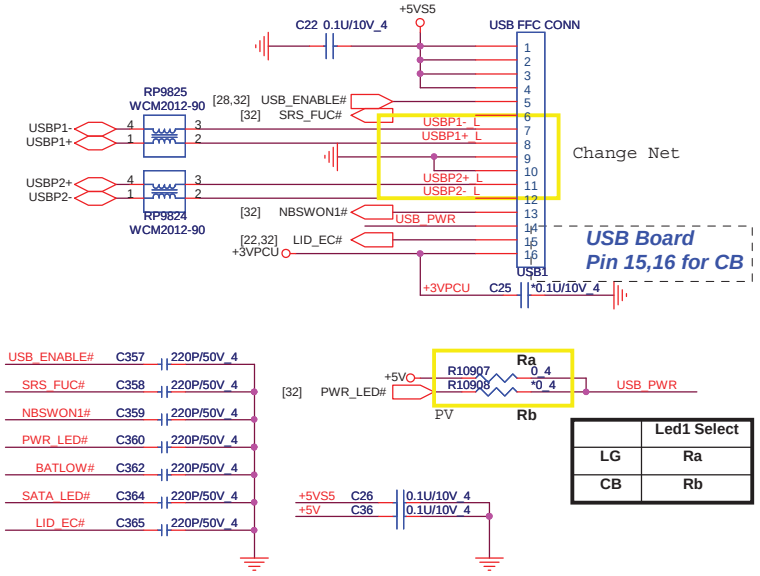
Size	Document Number	Rev
Custom	ODD/HDD/HOLES	3A

Date: Thursday, May 19, 2011 | Sheet 30 of 47

CPU FAN

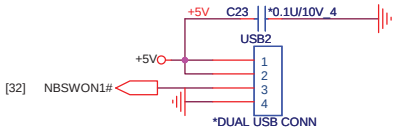


USB / Power LED & SW for 14"/15"/17" To USB Board



	Led1 Select
LG	Ra
CB	Rb

Power SW for 17"



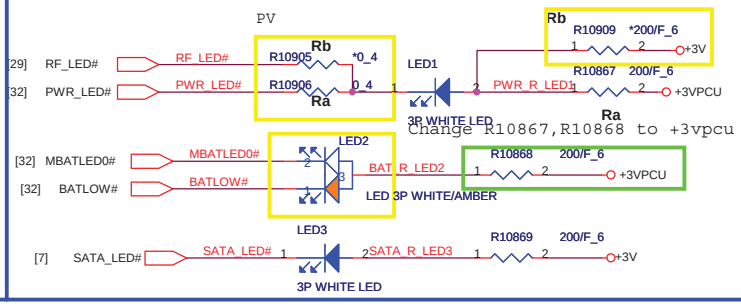
LED

Select Pin

	Led1 Select
LG	Ra
CB	Rb

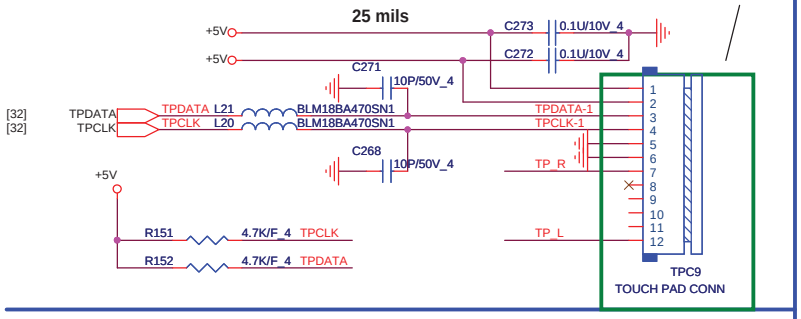
	Led2 P/N
LG	BEWH0051Z00
CB	BEWY0007ZA0

10 mils (250mA)

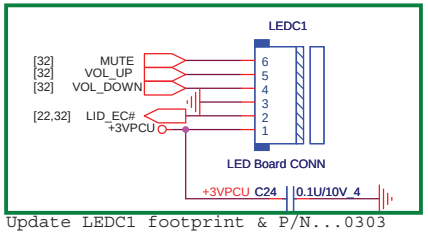


TOUCH PAD CONNECTOR To Click Board & FP

Update TPC9 footprint & P/N...0303

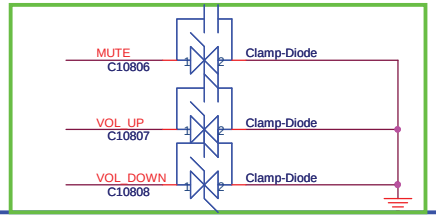


LID / MUTE / VU UP / VU DO To AD Function Board

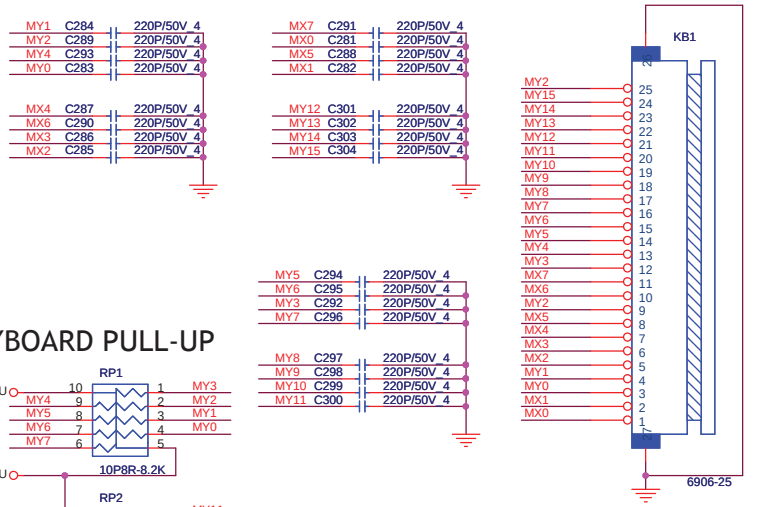


Update LEDC1 footprint & P/N...0303

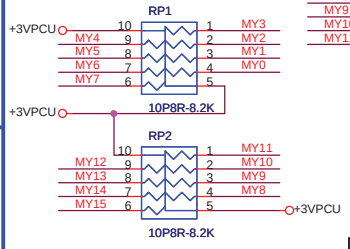
DV2 ...FOR EMI



KEYBOARD Con.

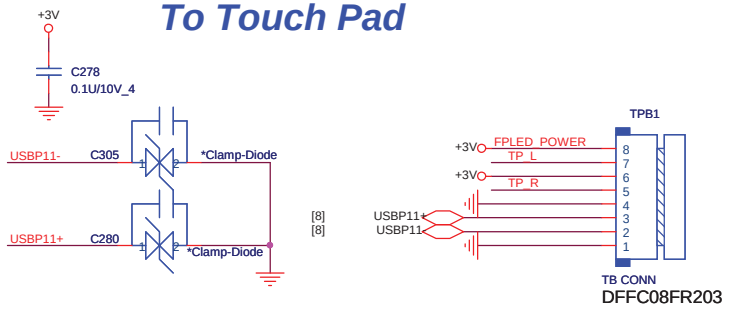


KEYBOARD PULL-UP

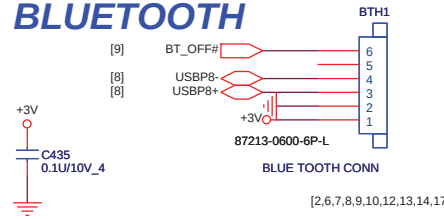


[32] MY[0..15]
[32] MX[0..7]
MY[0..15]
MX[0..7]

TP Button CONNECTOR To Touch Pad



BLUETOOTH



[6,7,10,17,21,22,23,25,29,30,41] +5V
[10,28,29,34,35,36,37,38,39,40,41,42,43] +5VS5
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,32,37,39,41,42] +3V
[7,22,32,33,34] +3VPCU

NB5

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/USB/eSATA	3A

Date: Wednesday, May 18, 2011 Sheet 31 of 47

DV2 ...FOR EMI

LAD0 C10809 *220P/50V_4
LAD1 C10810 *220P/50V_4
LAD2 C10811 *220P/50V_4
LAD3 C10812 *220P/50V_4
PLTRST# C10813 *220P/50V_4

+VCC_RTC R270 *0_4 +3V_ECACC L7001 BK1608HS220-T +3VPCU
C7008 1U/6.3V_4 C7009 1000P/50V_4
IT8502_AGND IT8502_AGND
+3V_STBY L7002 BK1608HS121-T +3VPCU
C7011 0.1U/10V_4
C7012 0.1U/10V_4 +3V +3VPCU R271 *0_4/S

+3V_RTC +VCC_RTC R7001 *0/short_4 C7010 0.1U/10V_4

+3VPCU 12 MILS C7002 0.1U/10V_4 C7003 0.1U/10V_4 C7004 0.1U/10V_4 C7005 0.1U/10V_4 C7006 0.1U/10V_4 C7007 0.1U/10V_4

Layout Note:
Place all capacitors close to IT8502N.

+3VPCU R7006 470K/J_4 EC_WRST C7013 0.1U/10V_4

Select Pin
Rb R8499 *10K_4 CB/LG Ra R8496 10K_4 +3VPCU

LG Select	
LG	Ra
CB	Rb

U7001

IT8518/CX

LPC: LAD0 LAD1 LAD2 LAD3 LPCRST#/WUI4/GPD2 LPCCLK LFRAME# LPCPD#/WUI6/GPE6
GPIO: GA20/GPB5 SERIRQ ECSMI#/GPD4 ECSCI#/GPD3 WRST# KBRST#/GPB6 PWUREQ#/BBO/GPC7 GPC0 TMA0/GPB2
PS/2: PS2DAT0/TMB1/GPF1 PS2CLK0/TMB0/GPF0 PS2DAT2/WUI21/GPF5 PS2CLK2/WUI20/GPF4
UART: DAC4/DCD0#/GPJ4 DSR0#/GPG6 GINT/CTS0#/GPD5 PS2DAT1/RTS0#/GPF3 DAC5/RIG0#/GPJ5 PS2CLK1/DTR0#/GPF2 RXD/SIN0/GPB0 TXD/SOUT0/GPB1
FLASH: GPG0 FSCK FMISO FMOSI FSCE# SSCE0#/GPG2
KBMX: KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15 KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7
CLOCK: CK32K CK32KE
VCC VSTBY VSTBY VSTBY VSTBY VSTBY VBAT AVCC VSTBY
EGCLK/WUI27/GPE3 EGCS#/WUI26/GPE2 EGAD/WUI25/GPE1 KSO16/SMOSI/GPC3 KSO17/SMISO/GPC5 L80HLAT/BAO/WUI24/GPE0 L80LLAT/WUI7/GPE7 SBUSY/GPG1/ID7 HMOSIGPH6/ID6 HMISO/GPH5/ID5 HSCK/GPH4/ID4 HSCE#/WUI19/GPH3/ID3 CTX1/WUI18/GPH2/SMDAT3/ID2 CRX1/WUI17/GPH1/SMCLK3/ID1 CLKRUN#/WUI16/GPH0/ID0
SMCLK2/WUI22/GPF6/PECI SMDAT2/WUI23/GPF7 SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2
PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/SSCK/GPA6 PWM7/GPA7 TACH0/GPD6 TACH1/TMA1/GPD7 TMR0/WUI2/GPC4 TMR1/WUI3/GPC6
PWRSW/GPE4 RI1#/WUI0/GPD0 RI2#/WUI1/GPD1 WUI5/GPE5 RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7
ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/WUI28/GPI4 ADC5/WUI29/GPI5 ADC6/WUI30/GPI6 ADC7/WUI31/GPI7
DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3
VSS VSS VSS VSS VSS VSS AVSS VCORE

IT8518E

BATLOW VRON [39] SLP_A# [6] EC_PWROK [6,17] SUSACK# [6] SUSON [35,41] SRS_FUC# [31] MBATLED0 H_SI R7002 *0_4/S PCH_SPI_SI [7] H_SO R7003 *0_4/S PCH_SPI_SO [7] H_CLK R7004 *0_4/S PCH_SPI_CLK [7] H_SCE# R7005 *0_4/S PCH_SPI_CS0# [7] MAINON [33,35,36,37,38,41] RF_LINK# [29] CLKRUN# [6,22]
EC_PECI_R R7014 *0_4/S EC_PECI [2]
SLP_SUS# [6] MBCLK [33] MBDATA [33] MBCLK2 [8,13,17] MBDATA2 [8,13,17]
For Battery charge/charge and cap board
For PCH SMB/DDR Thermal IC/VGA
LAN_POWER [41] T7008 AC_PRESENT [6] SATA5GP [9] SUS_PWR_ACK [3] VOLMUTE# [25] T7012
TACH_FAN_IN_R D7003 RB501-V-40 FAN1SIG [31]
3VS5_ON [34] SUSC# [6] 5VS5_ON [34]
NBSWON1# [31] LID_EC# [22,31] ACIN [33] SUSB# [6] PWR_LED
DGPU_PWROK [9,17,42,43] GFX_HWPG [39] SYS_I [33] AD_AIR [33] TEMP_MBAT [33] MUTE [31] VOL_UP [31] VOL_DOWN [31]
USB_CHR_C1 [28] GPU_PROCHOT [16] DNBSWON# [6] D7002 RB501-V-40 R181 10K/F_4 +3VS5

Led1 Select	
LG	non-stuff
CB	Rc

H_PROCHOT# Q R7061 *0_4/S H_PROCHOT# [2,39]
H_PROCHOT# EC Q7004 2N7002E R7017 100K/J_4
+3VPCU R7013 10K/J_4 NBSWON1# C7014 0.1U/10V_4
Rc MBATLED0# [31] MBATLED0 Q9023 *2N7002
PWR_LED# [31] PWR_LED Q38 2N7002E
BATLOW# [31] BATLOW Q40 2N7002E

thermal shutdown circuit

EC_WRST EC_CT_UP R130 *4.7K/F_4 +1.05V_VTT C238 220P/50V_4 PV Change PM_THRMTRIP# [2,9] Q14 *MMBT3904-7-F

0330....add FAN PWM control at pin30
R10894 *0_4/S FAN_PWM [31]

MBCLK R7009 10K/J_4
MBDATA R7007 10K/J_4
SRS_FUC# R7016 10K/J_4
TPCLK R7011 *10K/J_4
TPDATA R7012 *10K/J_4
MBCLK2 R7010 10K/J_4
MBDATA2 R7008 10K/J_4
TACH_FAN_IN_R R10185 10K/F_4
MUTE R10896 10K/J_4
VOL_UP R10897 10K/J_4
VOL_DOWN R10898 10K/F_4

0330....audio function button need add pull-high Res

D5 need to close PCH.
ACZ_SDOUT TP9040 GPIO33_E_R EC_DEBUG1 D5 RB501V-40
USB_ENABLE# EC_SCK EC_SCK_L SBY100505T-121Y-N L8042 C10822 22P_50v
EJECT# MY[0..15] MX[0..7]
EC_SO EC_SI EC_CE#
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15
MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7
PCH_SUSCLK R7020 *0/J_4 EC_CK32K *0_4/S R331
L7000 BK1608HS121-T IT8502_AGND
C7015 0.1U/10V_4

DV2
add DGPU_PWROK for muxless no thermal
FOR UMA R7015 *10K/J_4 DGPU_PWR_EN [9,42,43]

SPI FLASH EN25Q32B-104HIP: AKE39ZN0Q02
MX25L3206EM2I-12G: AKE39FP0Z02
Socket: DG008000031
U7002 CE# SCK SI SO WP# VSS HOLD# VDD
EC_CE# EC_SCK R7023 47/J_4 EC_SCK_R EC_SI R7024 47/J_4 EC_SI_R EC_SO R7025 15/J_4 EC_SO_R
R7027 10K/J_4 R7026 10K/J_4 C7018 0.1U/10V_4
EC_SCK_R R10910 47_4 C10823 22P
SPI Flash Socket

[6,7,10] +3V_RTC
[2,6,7,8,9,10,27,29,34,37,38,41,43] +3VS5
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,37,39,41,42] +3V
[7,22,31,33,34] +3VPCU

NB5

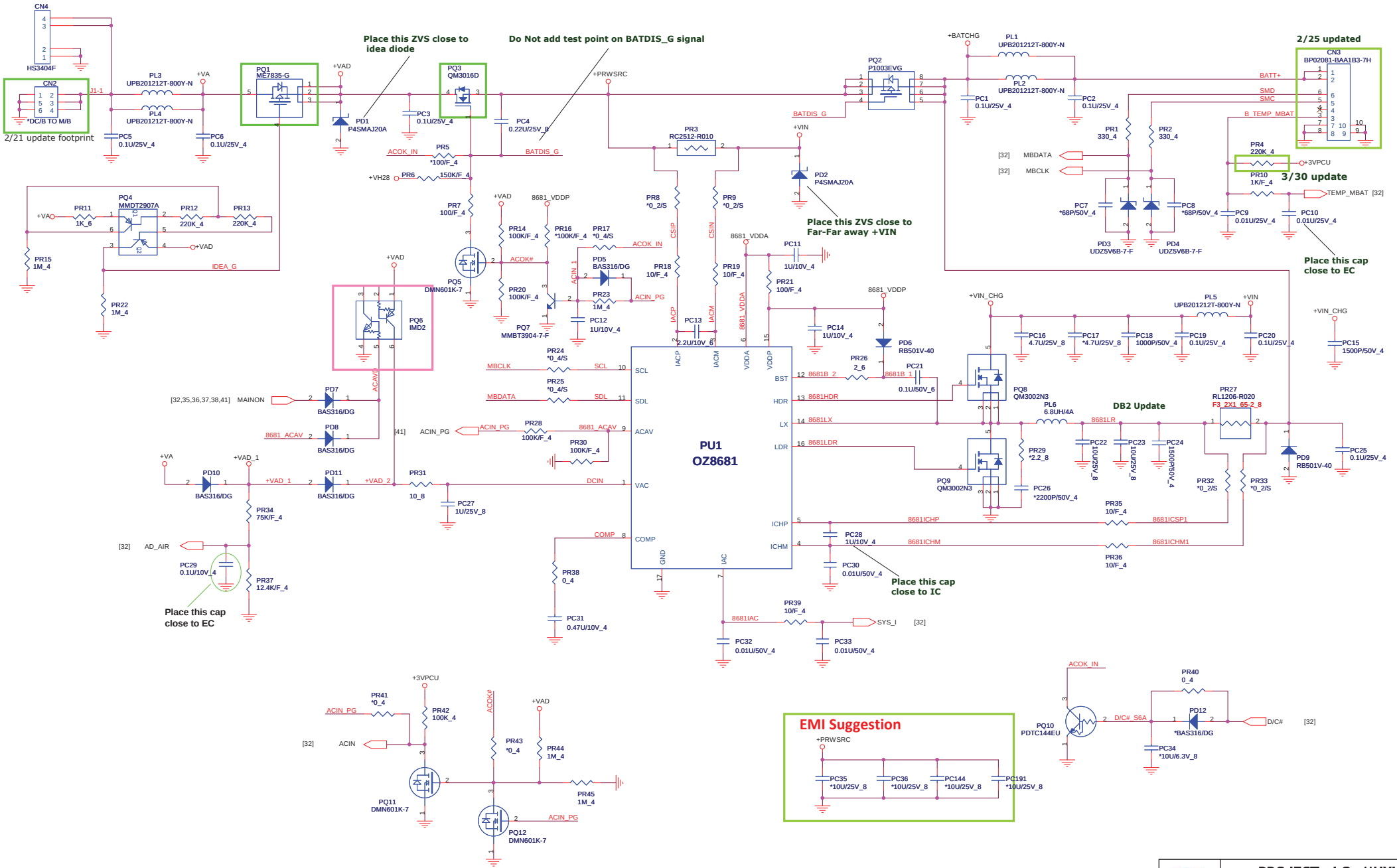
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IT8515/CX/FLASH	3A

Date: Friday, May 20, 2011 Sheet 32 of 47

LG2_DIS only

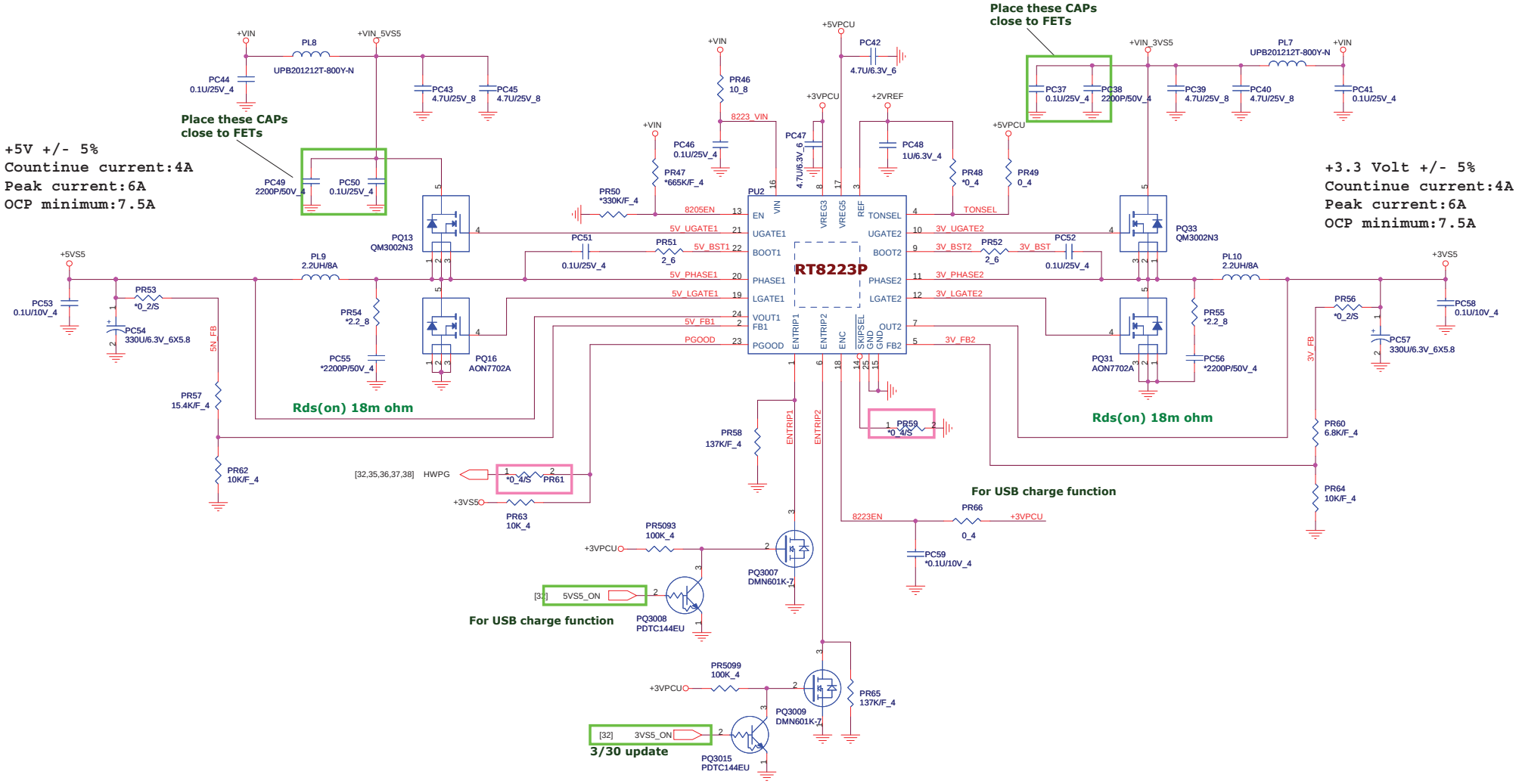
TOP DC_JACK
90W/120W(QC)



PROJECT : LGx MUXLESS	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Charger (OZ8681)
Rev: 2A	
Date: Thursday, May 19, 2011	Sheet 33 of 46

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

LG2_DIS only



NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VS5 (RT8223M)	Rev: 2A
Date: Wednesday, May 18, 2011	Sheet 34 of 47	

LG2_DIS only

(VTT/2A)

+0.75V_DDR_VTT

PC60 10U/6.3V_8
PC61 10U/6.3V_8

PU3
RT8207LGQW

1 VTTGND
2 VTTSNS
3 GND
4 MODE
5 VTTREF
6 COMP
7 NC
8 VDDQSNS
9 VDDQSET
10 S3
11 S5
12 NC
13 PGOOD
14 V5FILT
15 V5IN
16 8207CS
17 CS_GND
18 PGND
19 8207DRVL
20 8207LX
21 8207DRVH
22 8207BST
23 VLDOIN
24 VTT
25 GND

+1.5VSUS
PC67 *0.1U/50V_6

PR67 *0_4
PR69 0_4
8207MOD

PR68 2_6
8207BSTR
PC68 0.1U/25V_4

(3mA)
[4,12,13] DDR_VTTREF
PC69 0.033U/10V_4
V5FILT

RILIM = ILIM x RDS(ON) / 10uA

PR72 7.5K/F_4
+5VS5
PC73 1U/6.3V_4

8207S3
PR73 *0_4/S
[32,41] SUSON
8207S5

+VIN_DDR
8207TON
PR75 619K/F_4

PC74 1U/6.3V_4
PR74 10_6

PR76 *0_4/S
DDRPG
HWPG [32,34,36,37,38]

PQ17 QM3002N3
PQ18 AON6790

PR70 *2.2_8
PC72 *2200P/50V_4

RDSon=4.7m ohm

+VIN_DDR
PC62 0.1U/25V_4
PC63 4.7U/25V_8
PC64 4.7U/25V_8
PC65 2200P/50V_4
PL11 UPB201212T-800Y-N
+VIN
PC66 0.1U/25V_4

PL12 1UH/15A

+1.5VSUS +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

+1.5VSUS
PC70 0.1U/10V_4
PC71 390U/2.5V_6X5.8ESR10
PR71 *0_2/S

Place this short pad close to output CAP

1.5VSUS_FB
PR77 10K/F_4
8207FB
PR78 10K/F_4

Place this FB parts close to IC

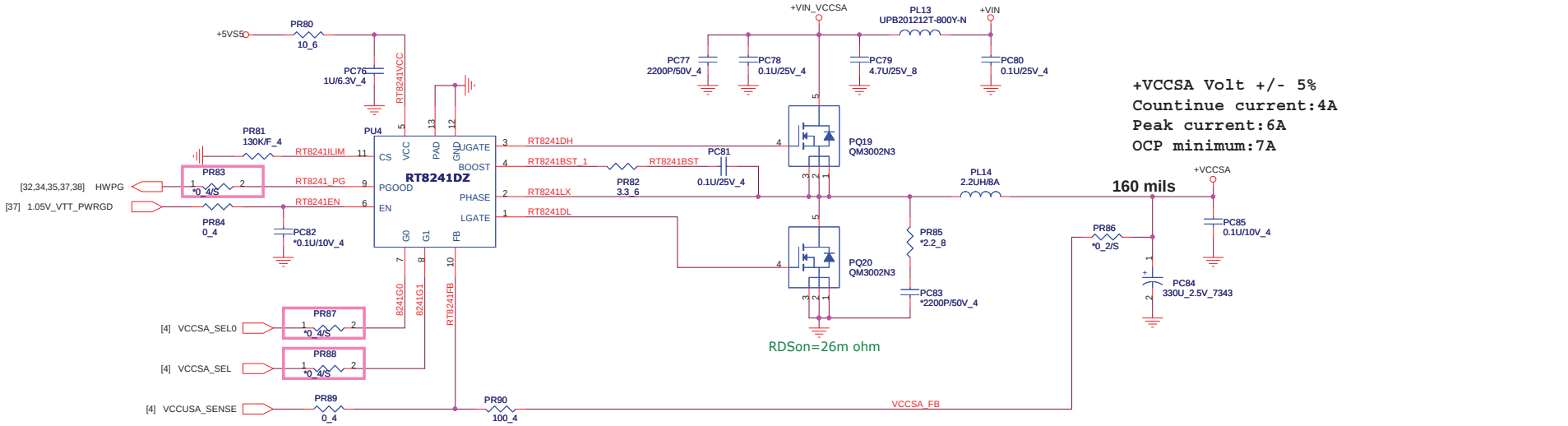
PD13
RB501V-40
MAINON [32,33,36,37,38,41]
PC75 0.1U/10V_4
PR79 100K/F_4

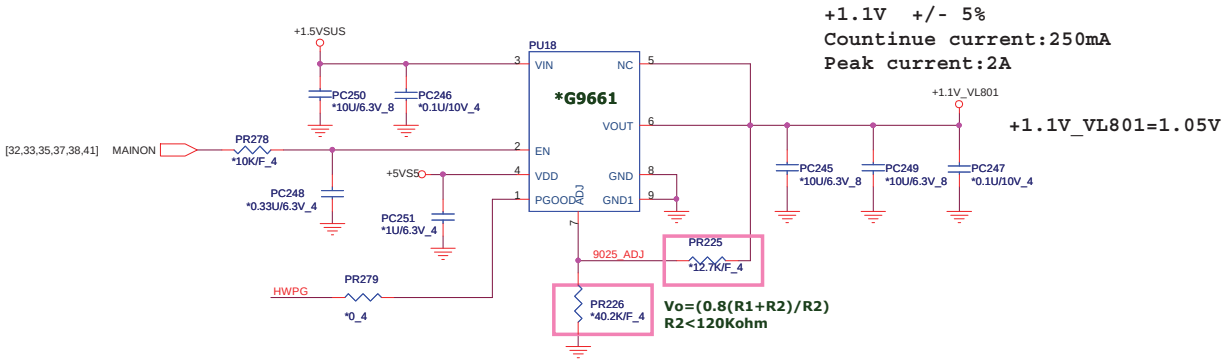
[12,13,41] +0.75V_DDR_VTT
[2,4,12,13,36,43] +1.5VSUS
[10,28,29,31,34,36,37,38,39,40,41,42,43] +5VS5
[22,26,29,33,34,36,37,40,41,42,43] +VIN

NB5

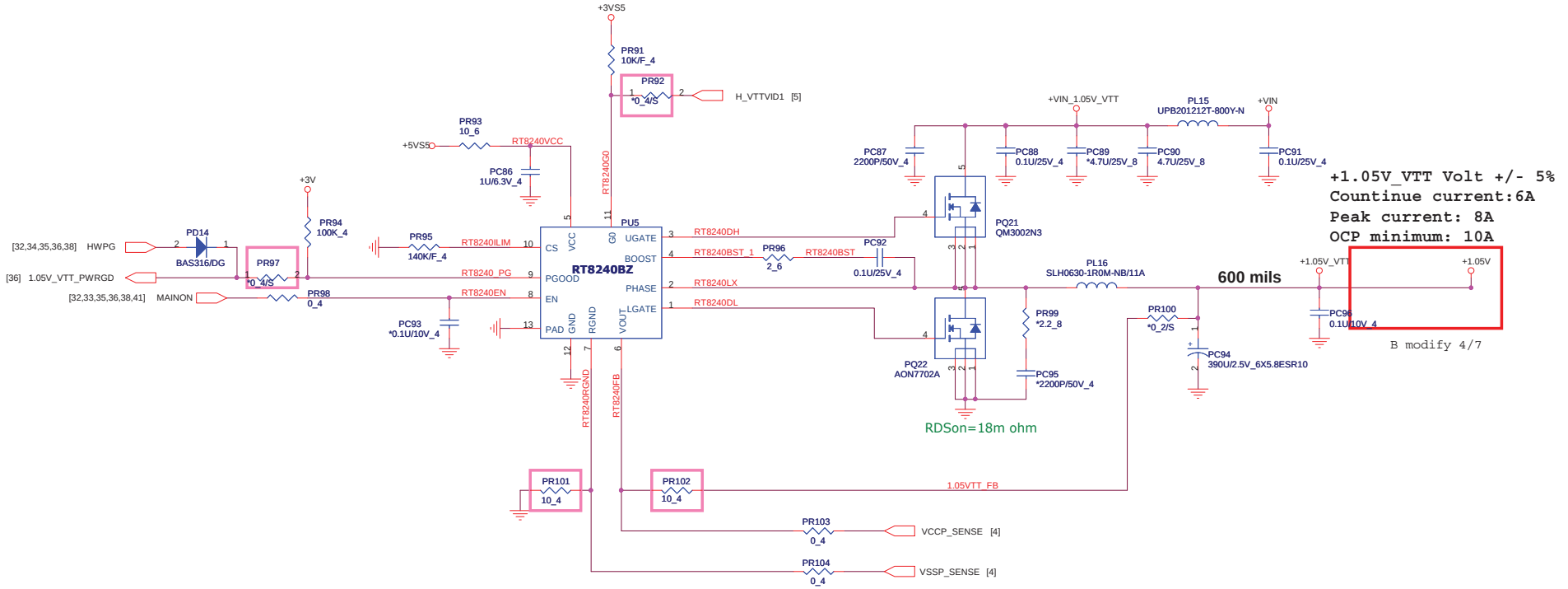
PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	2A
Date: Wednesday, May 18, 2011	Sheet 35 of 47	



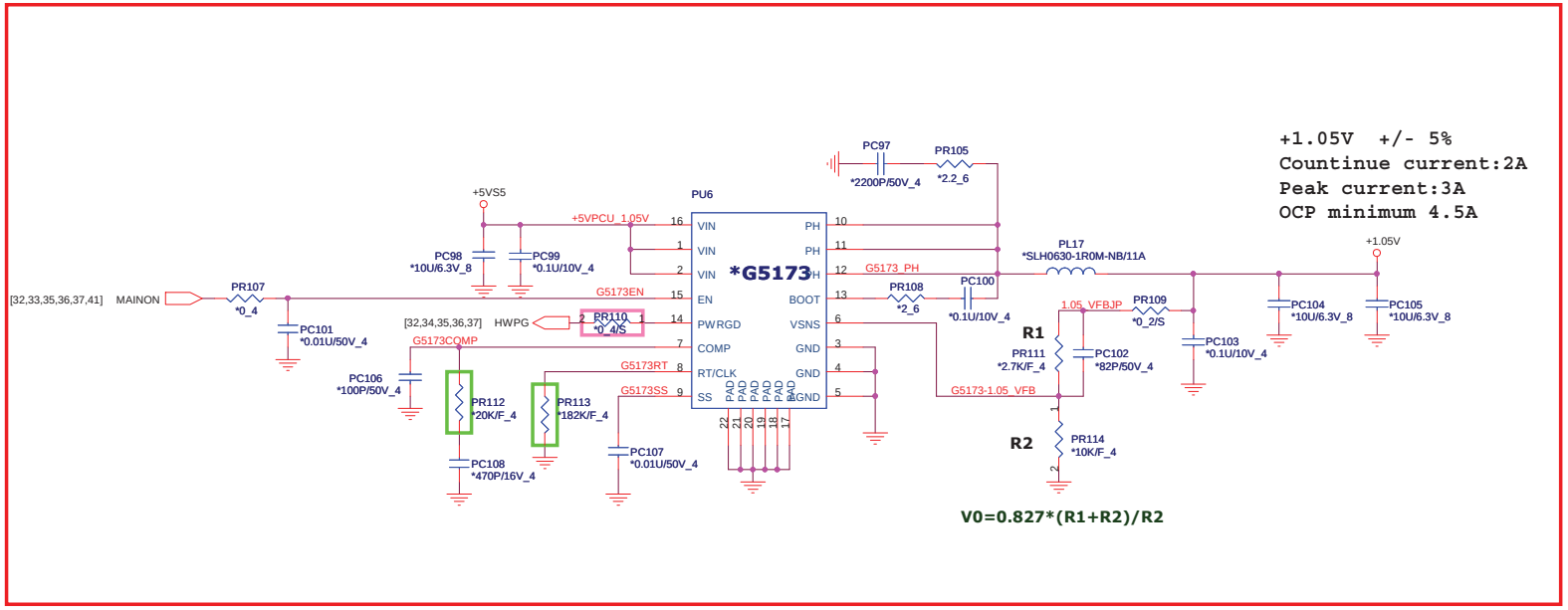


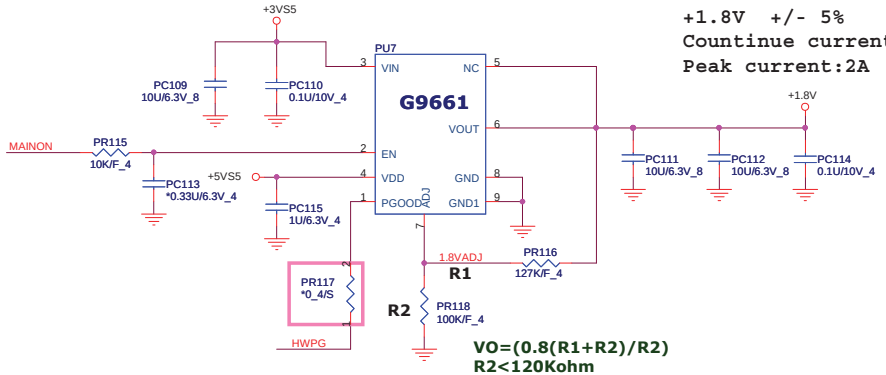
NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: VCCSA (RT8241A)	Rev: 2A
Date: Thursday, May 19, 2011	Sheet 36 of 47	



NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: Custom	Document Number: +1.05V_VTT(RT8240B)	Rev: 2A
Date: Wednesday, May 18, 2011	Sheet 37 of 46	

B modify 4/7





NB5

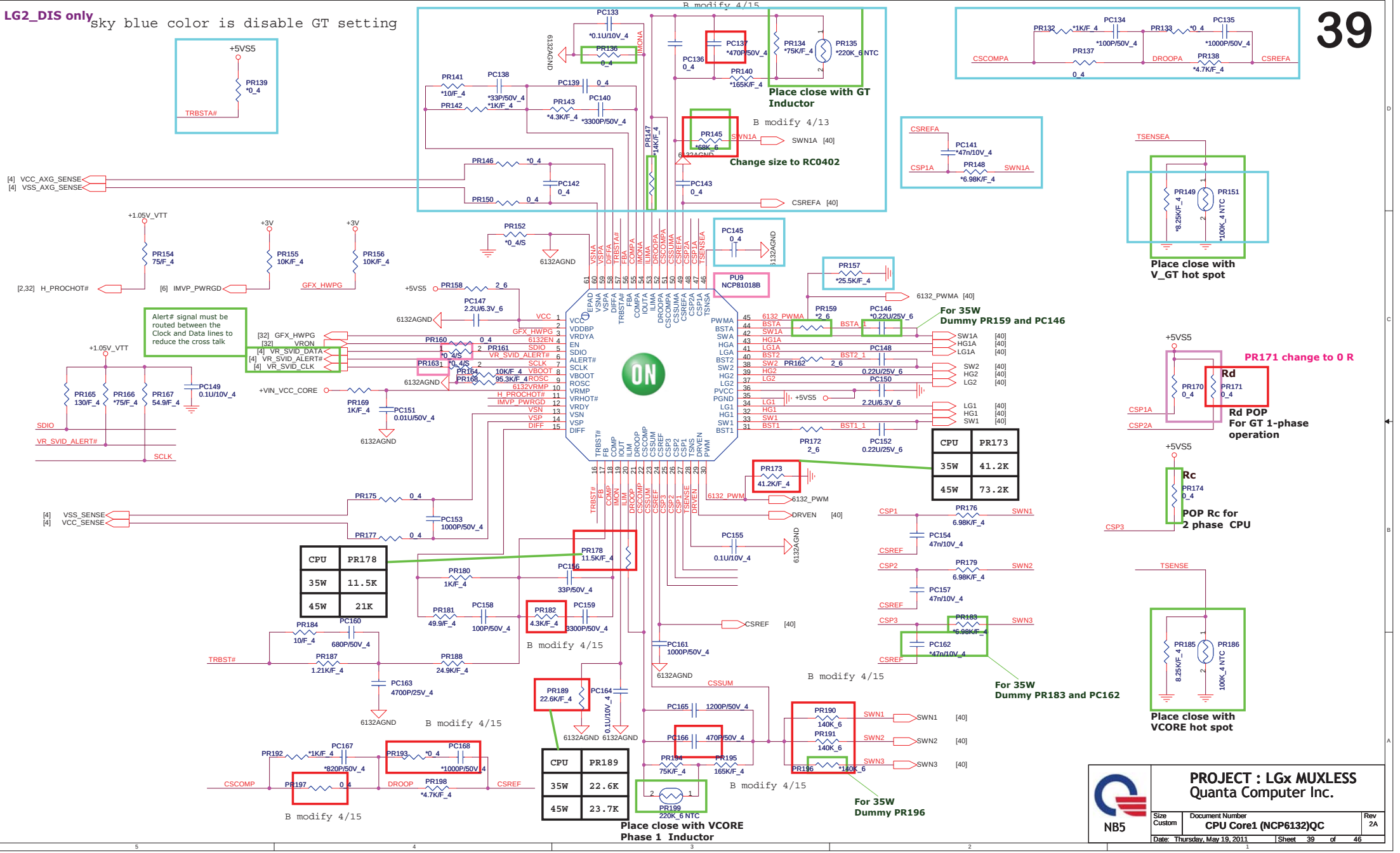
PROJECT : LGx MUXLESS
Quanta Computer Inc.

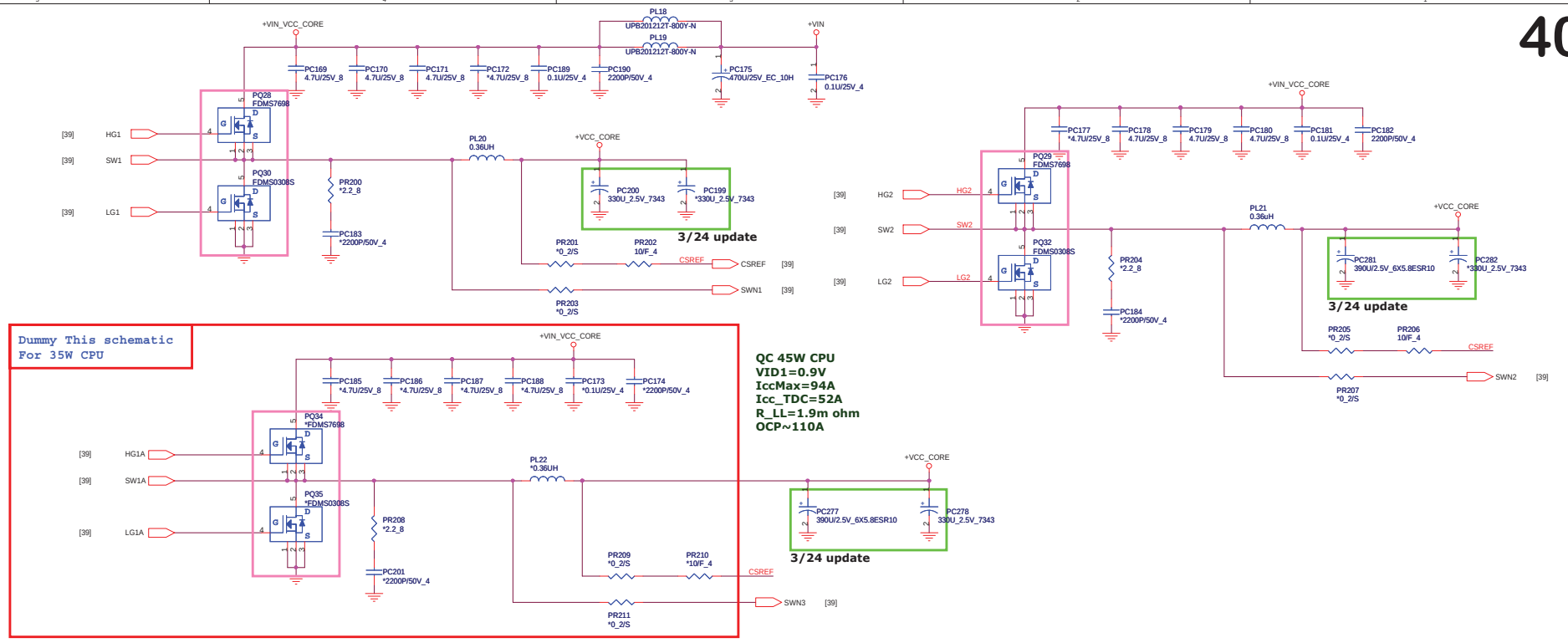
Size	Document Number	Rev
Custom	+1.05V/+1.8V (G5173)	2A

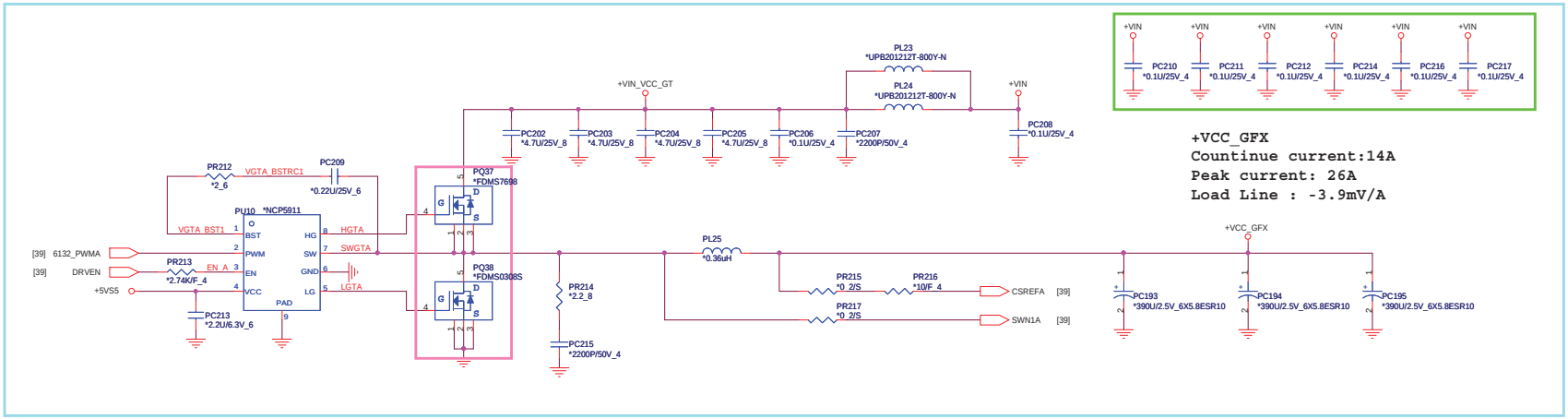
Date: Wednesday, May 18, 2011 Sheet 38 of 47

LG2_DIS only

sky blue color is disable GT setting

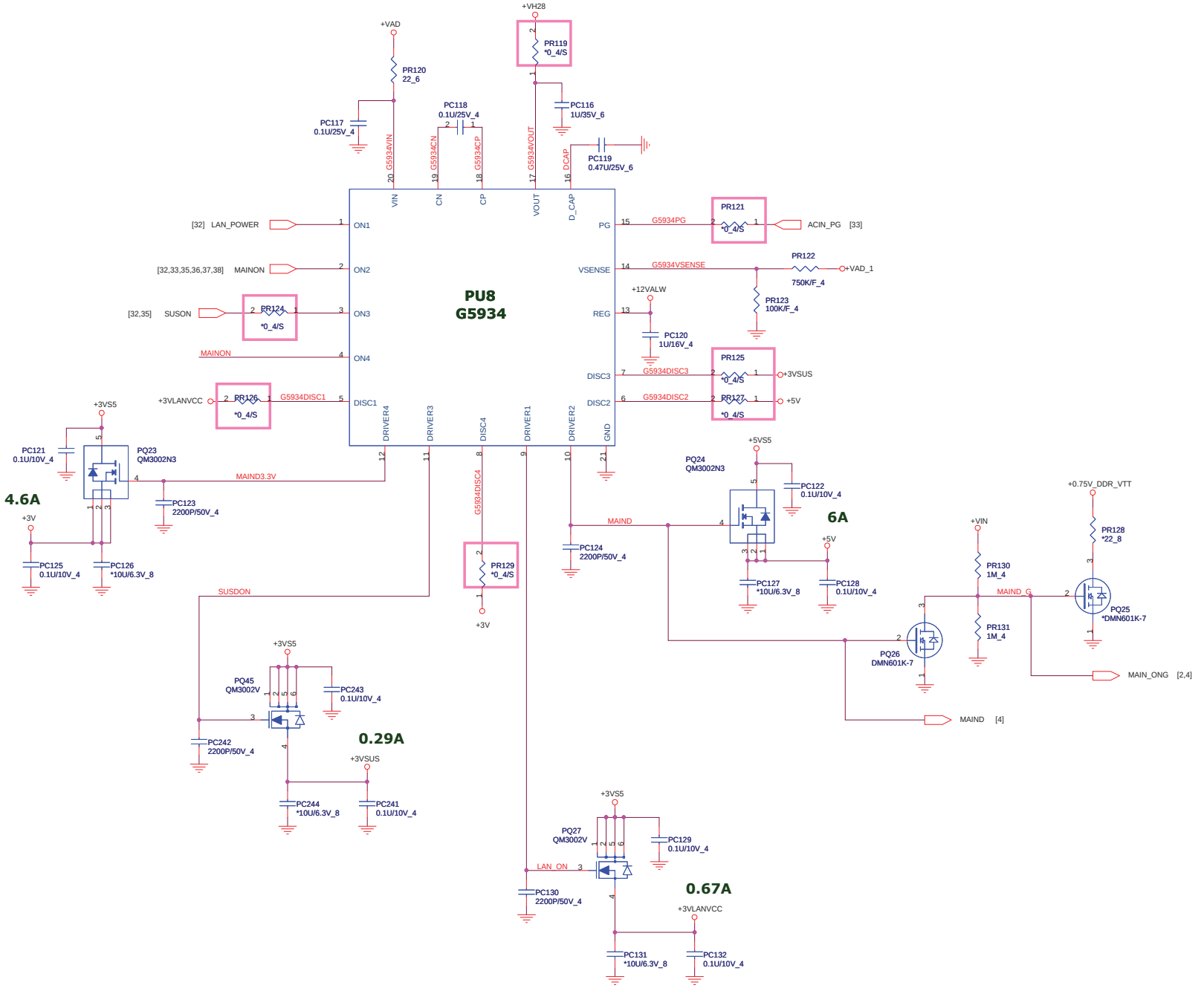






sky blue color is disable GT setting

NB5	PROJECT : LGx MUXLESS Quanta Computer Inc.	
Size: C	Document Number: CPU Core2 (NCP5911)QC	Rev: 2A
Date: Wednesday, May 18, 2011	Sheet 40 of 46	



[12,13,35] +0.75V_DDR_VTT
[27] +3VLANVCC
[2,4,12,13,35,36,43] +1.5VSUS
[33] +BATCHG
[30,43] +12VALW
[10,28,29,31,34,35,36,37,38,39,40,42,43] +5VS5

[2,6,7,8,9,10,27,29,32,34,37,38,43] +3VS5
[33] +VAD_1
[33] +VH28
[4,7,10,38] +1.8V
[22,26,29,33,34,35,36,37,40,42,43] +VIN
[6,7,10,17,21,22,23,25,29,30,31] +5V
[33] +VA

NB5

PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	2A

Date: Wednesday, May 18, 2011 | Sheet 41 of 47

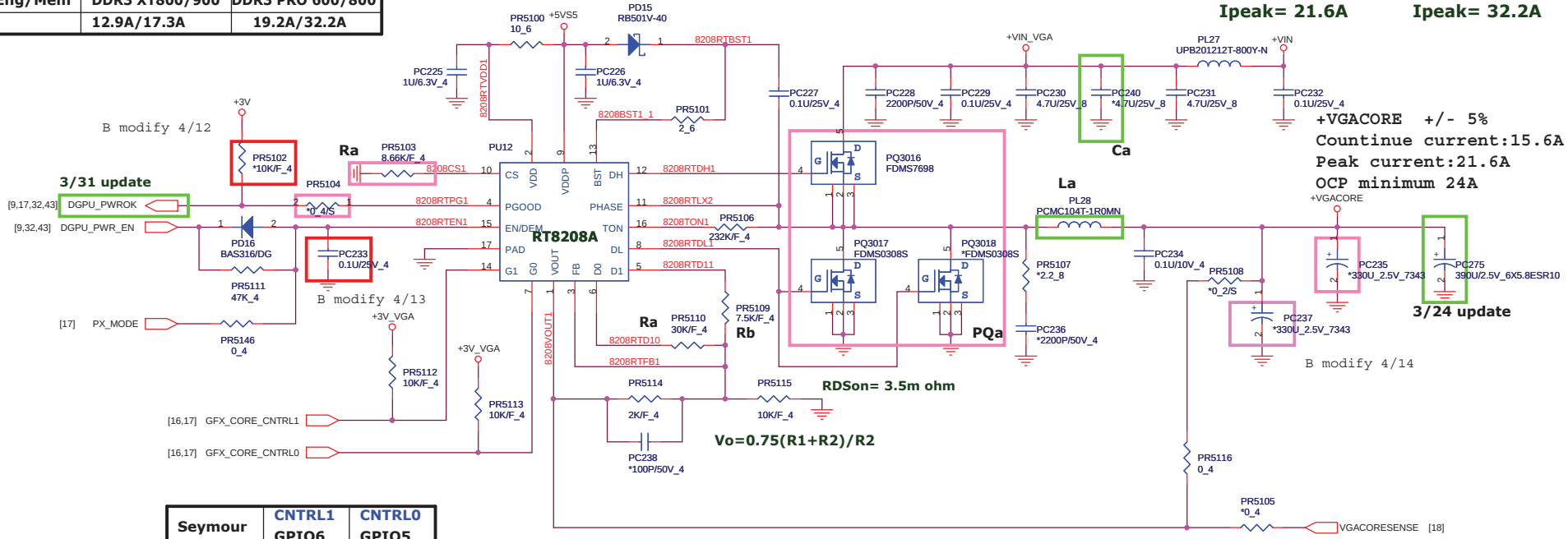
VGA Core

LG2_DIS only
VGA chip only Seymour

	Seymour (OCP 24A)	Whistler
Ca	PC240 X	V
Cb	PC235 PC237 X	V
PQa	PQ3018 X	V
La	1U/15A	0.45U25A
Ra	8.66K-ohm	8.66K-ohm
Eng/Mem	DDR3 XT800/900	DDR3 PRO 600/800
	12.9A/17.3A	19.2A/32.2A

Seymour-XT 64bit
Irms= 15.6A
Ipeak= 21.6A

Whistler
Irms= 19.2A
Ipeak= 32.2A



Seymour	CNTRL1 GPIO6	CNTRL0 GPIO5	
0.9V	0	0	
0.95V	0	1	
1.1V	1	0	
1.15V	1	1	default

Whistler	CNTRL1 GPIO6	CNTRL0 GPIO5	
0.9V	0	0	
1.0V	0	1	Ra --> 15K-ohm
1.05V	1	0	Rb --> 10K-ohm
1.15V	1	1	

[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41] +3V
+3V_GFX
[10,28,29,31,34,35,36,37,38,39,40,41,43] +5VSS
[17,18] +VGACORE
[22,26,29,33,34,35,36,37,40,41,43] +VIN

NB5

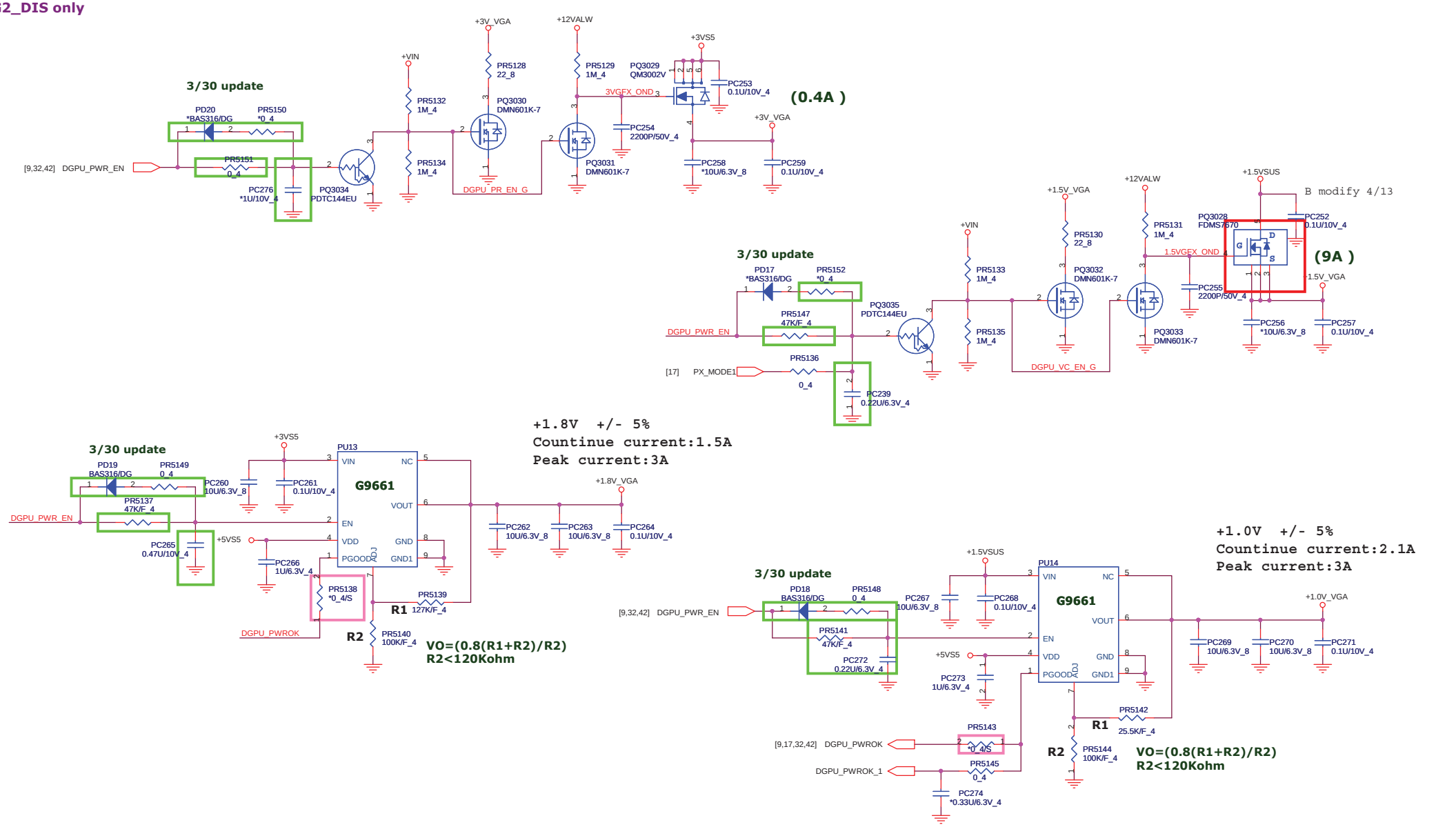
PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208)	2A

Date: Wednesday, May 18, 2011 | Sheet 42 of 46

VGA Core

LG2_DIS only

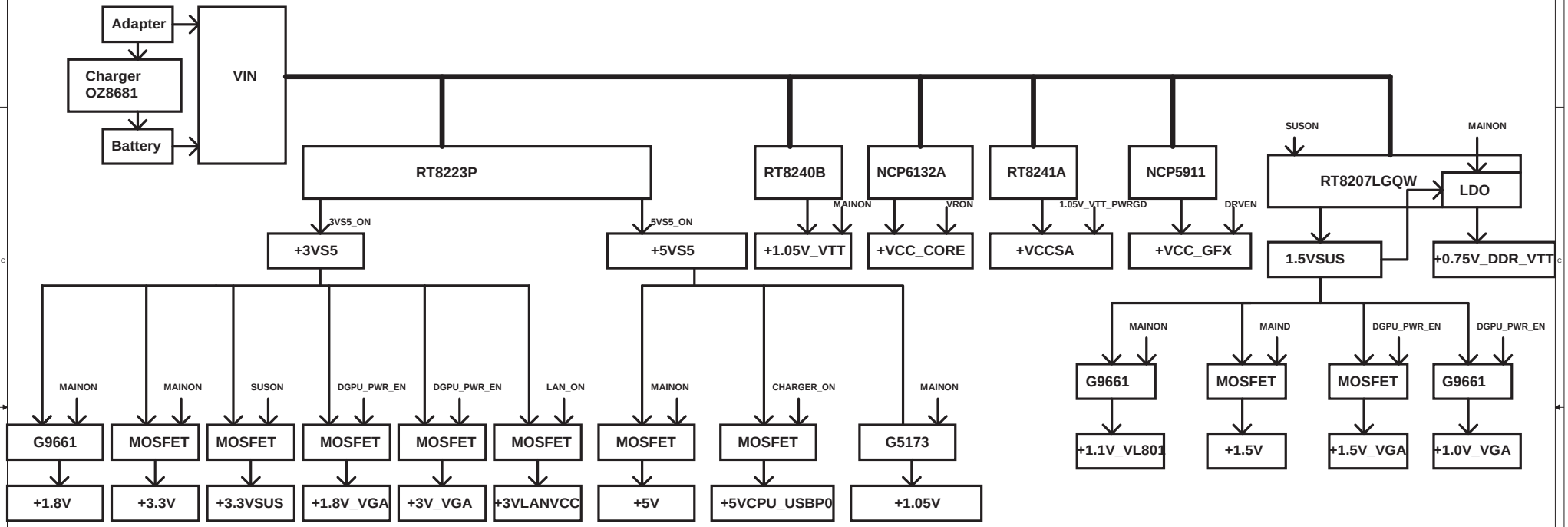


NB5

PROJECT : LGx MUXLESS
Quanta Computer Inc.

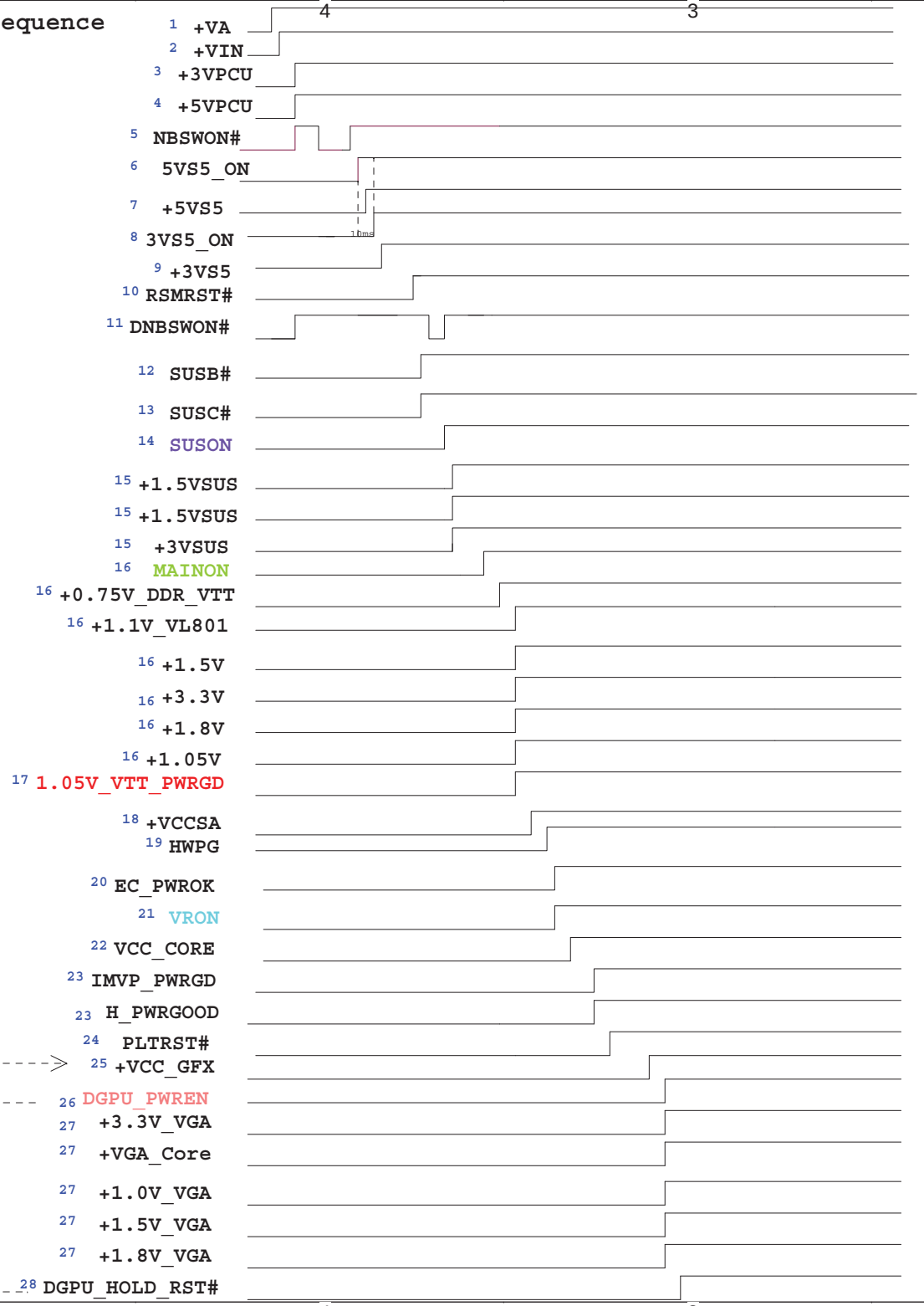
Size	Document Number	Rev
Custom	+VGA POWER	2A
Date: Thursday, May 19, 2011	Sheet 43 of 47	

LG2/4
Power rail map



NB5	PROJECT : LG2/4 DIS Quanta Computer Inc.	
Size	Document Number Power Block Diagram	Rev 3A
Date: Wednesday, May 18, 2011	Sheet 44 of 47	

LG2/4/6 Power Sequence



UMA/Muxless internal GPU Sequence

DIS GPU Power Sequence

NB5	PROJECT : LG2/4 DIS Quanta Computer Inc.		
	Size	Document Number Power Sequence	Rev 3A
	Date:	Sheet 45 of 47	