Model Name : P5WE0
File Name : LA-6901P
BOM P/N:43

Compal Confidential

P5WE0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P GS/GV

2010-08-11

REV:0.1

Compal Electronics, Inc.			
Title	Cover Page		
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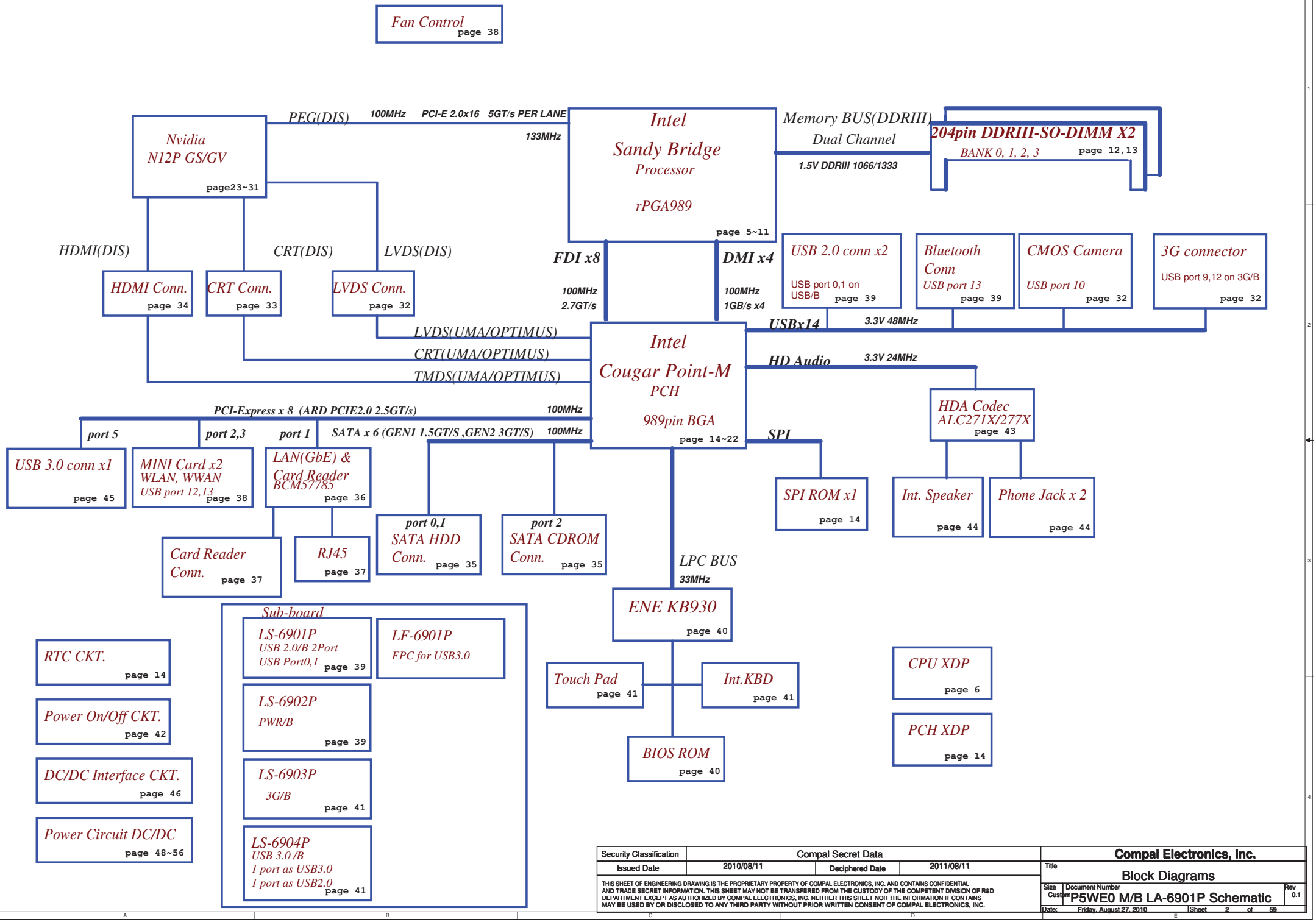

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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT & USB30 & USB20 Config

3G SKU: 3G@ USB30 SKU: USB30@ OPTMIUS SKU: OPT@

BT SKU: BT@ USB20 SKU: USB20@ Non-OPTMIUS SKU: NOPT@

LAN Chip A0 version: A0@

LAN chip B0 Version: B0@

BOM Config

UMA Only: BT@/3G@/USB30@/UMA@/UMAO@/NOPT@/A0@

OPTIMUS: BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@

DIS Only: BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@

VRAM BOM Config

X76***BOL01: Samsung

X76***BOL02: Hynix

VRAM P/N :

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT
DVT
PVT
Pre-MP

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
	UHCI1	2	USB 2.0 & USB3.0 Conn.
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card 1(WLAN)
		9	3G/B(WWAN)
	UHCI5	10	Camera
		11	Mini Card 2(Reserved)
	UHCI6	12	SIM Card (3G/B)
		13	Blue Tooth

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Title: Notes List

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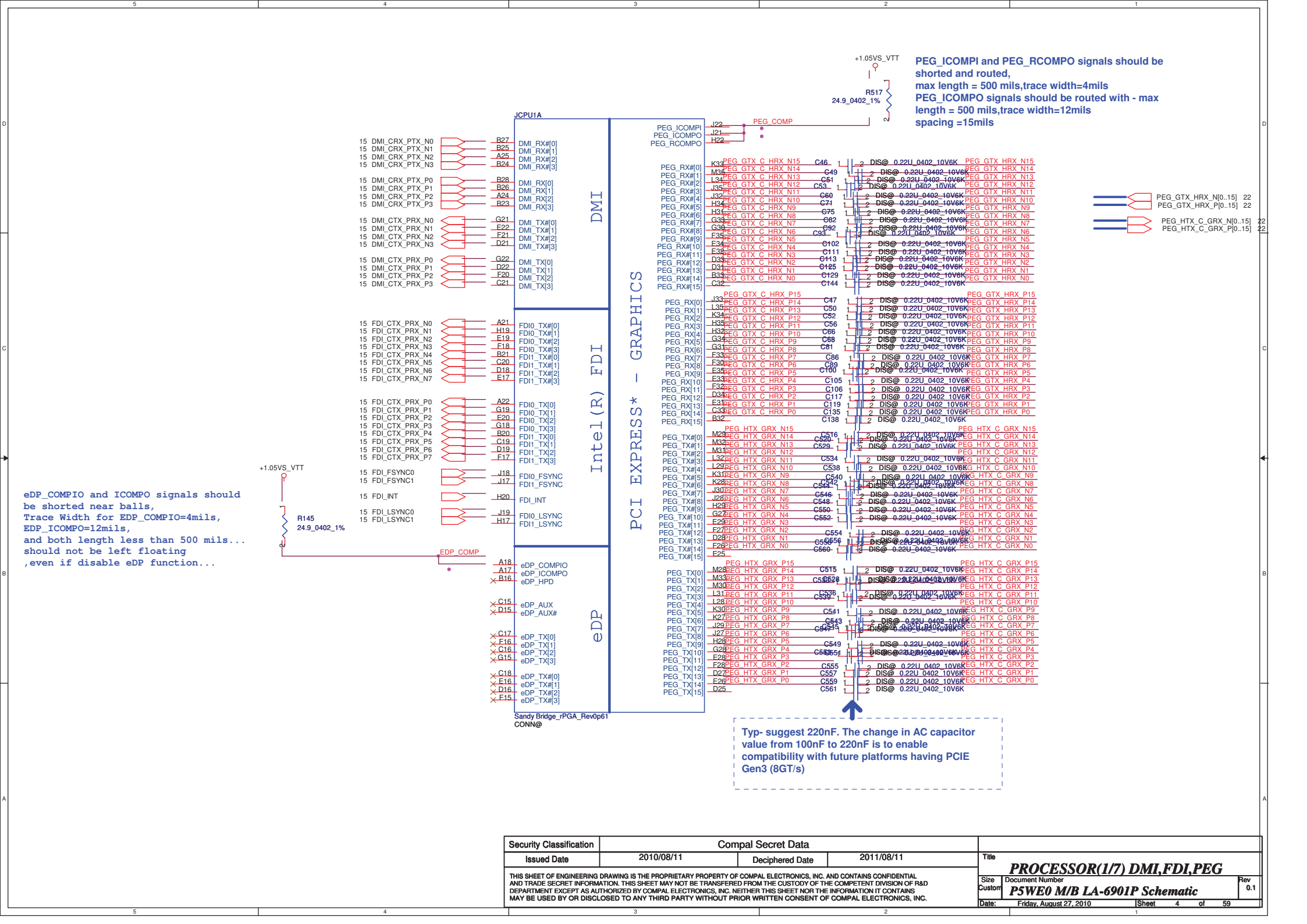

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Title	PROCESSOR(1/7) DMI,FDI,PEG		
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic		Rev: 0.1
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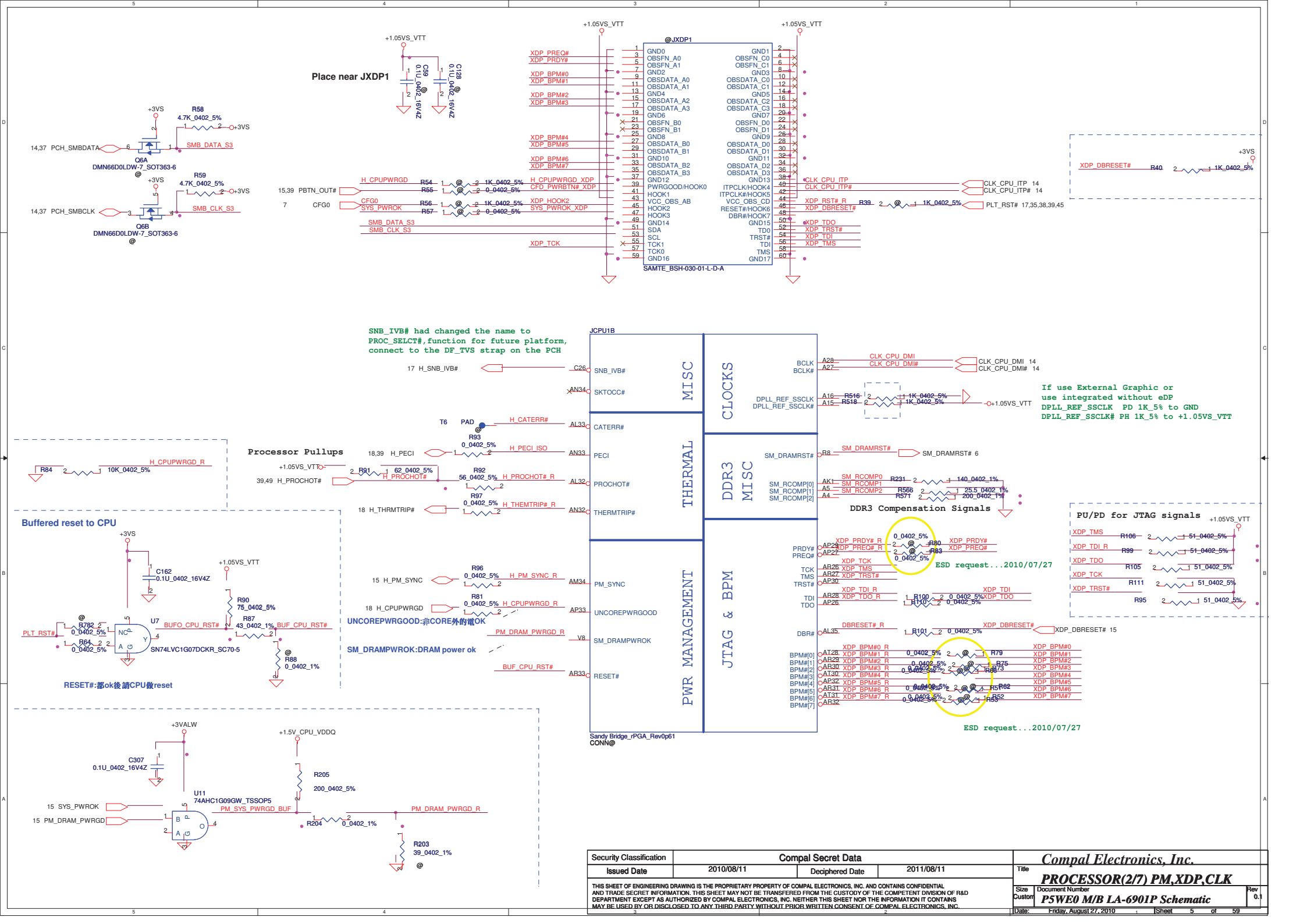

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Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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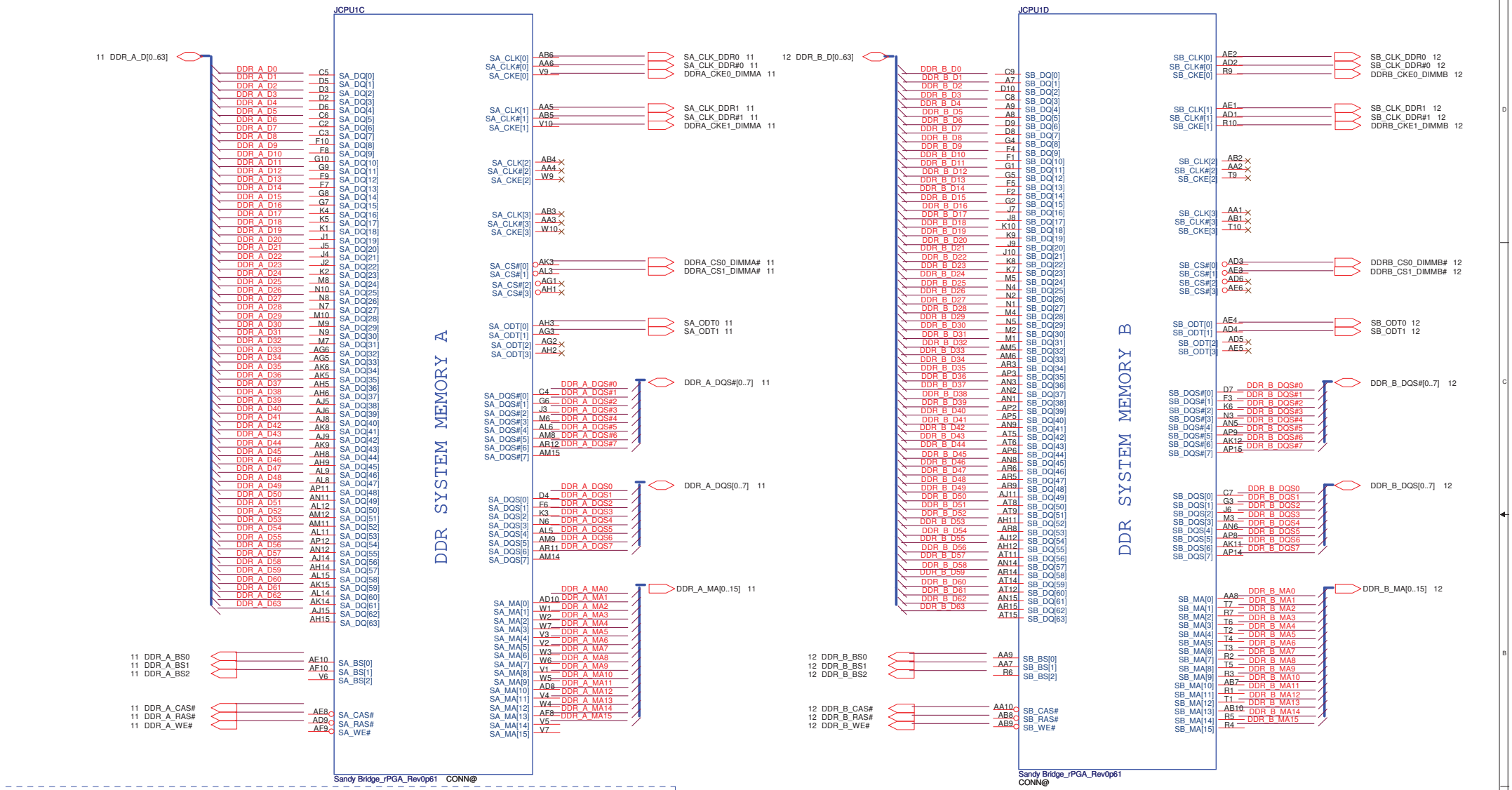

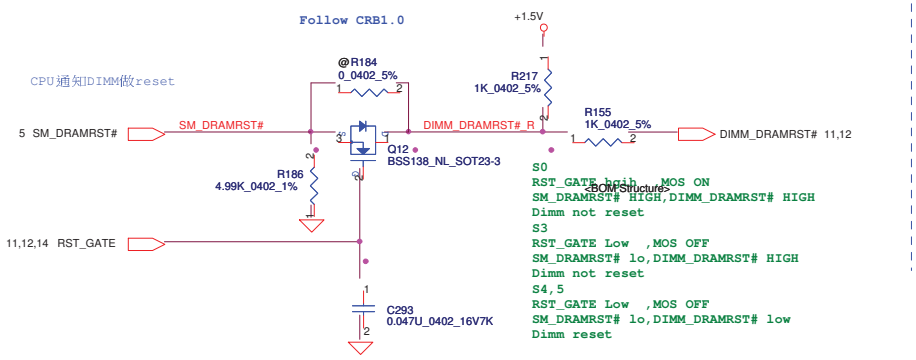

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Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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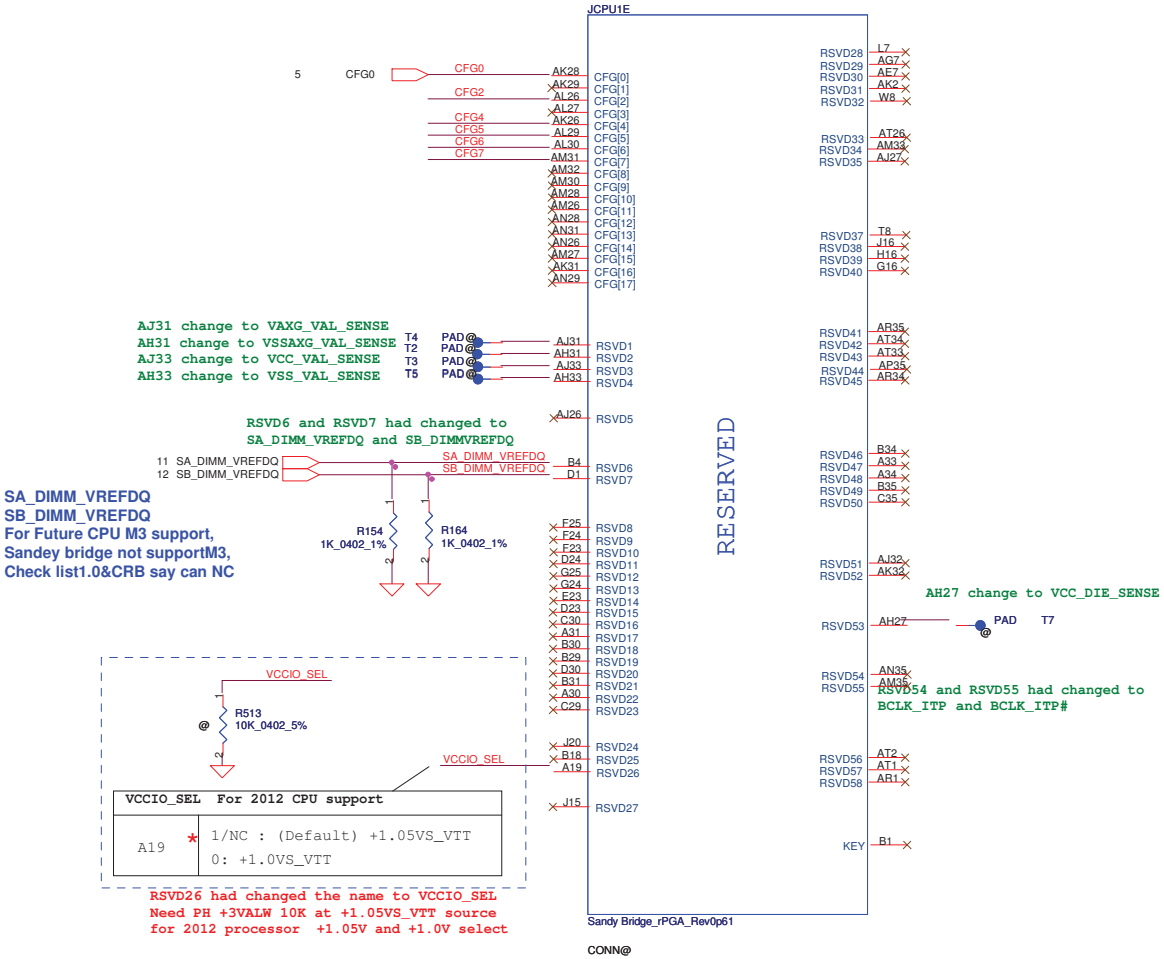
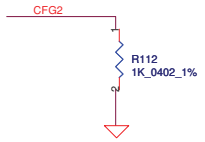
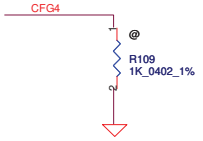
CFG Straps for Processor

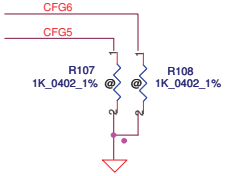




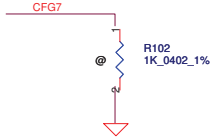
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

SV type CPU

QC 94A
DC 53A

JCPU1F

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

8.5A

+CPU_CORE

+1.05VS_VTT

INTEL Recommend
4*470uF,16*22uF and 10*10uF
from PDDG 1.0

INTEL Recommend
2*330uF,12*22uF
from PDDG 1.0

Follow Power Suggestion ,
place 3-pin Cap for CPU_CORE

PAW00
use 470uF*2
330uF*3

Place the PU
resistors close to VR

Place the PU
resistors close to CPU

VSSIO_SENSE
change to
VSS_SENSE_VCCIO

Should change to connect form
power cirucit & layout differential
with VCCIO_SENSE.

Sandy Bridge rPGA_Rev0p61

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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POWER

INTEL Recommend
2*470uF,12*22uF
from PDDG 1.0

QC 33A
DC 26A

+VGFX_CORE

R151
0_0402_5%
DISO@

UMA@ 22U_0805_6.3V6M: C611, C625, C212, C272, C211, C231
UMA@ 22U_0805_6.3V6M: C210, C209, C274, C271, C242, C275
UMA@ 330U_D2_2V_Y: C646, C645
UMA@ 22U_0805_6.3V6M: C208, C273, C600, C599

JCPU1G

GRAPHICS
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

SENSE LINES
VAXG_SENSE AK35 → VCC_AXG_SENSE 54
VSSAXG_SENSE AK34 → VSS_AXG_SENSE 54

VREF
SM_VREF AL1
+V_SM_VREF should have 20 mil trace width
+1.5V_CPU_VDDQ
R582 100_0402_1%
R575 100_0402_1%
C688 0.1U_0402_16V4Z
<BOM Structure>

DDR3 -1.5V RAILS
10A
VDDQ1 AF7, VDDQ2 AF4, VDDQ3 AF1, VDDQ4 AC7, VDDQ5 AC4, VDDQ6 AC1, VDDQ7 Y7, VDDQ8 Y4, VDDQ9 Y1, VDDQ10 U7, VDDQ11 U4, VDDQ12 U1, VDDQ13 P7, VDDQ14 P4, VDDQ15 P1
+1.5V_CPU_VDDQ
10U_0805_6.3V6M: C383, C384, C382, C381, C385, C361
330U_D2_2V_Y: C355
J1 PAD-OPEN 4x4m @ (+1.5V)
J2 PAD-OPEN 4x4m @ (+1.5VS)
Short for +1.5VS to +1.5V_1
INTEL Recommend
1*330uF,6*10uF
from PDDG 1.0

INTEL Recommend
1*330uF,3*10uF
from PDDG 1.0

SA RAIL
6A
VCCSA1 M27, VCCSA2 M26, VCCSA3 L26, VCCSA4 J26, VCCSA5 J25, VCCSA6 J24, VCCSA7 H26, VCCSA8 H25
+VCCSA
10U_0805_6.3V6M: C603, C214, C605
10U_0603_6.3V6M: C219, C213
330U_D2_2V_Y: C221
R137 0_0402_5% VCCSA_SENSE
If possible,use os-con cap
if not,use the D2 size
R141 0_0402_5% VSSSA_SENSE 51

MISC
VCCSA_SENSE H23 → VCCSA_SENSE 51
VCCSA_VID0
VCCSA_VID1
FC_C22 C22
C24
VCCSA_VID1 → VCCSA_VID1 51
FC_C22 change to VCCSA_VID0
R143 10K_0402_5%
R138 @0_0402_5%

VCCSA				
VID0	VID1	Vout	2011CPU	2012CPU
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

1.8V RAIL
1.2A
+1.8VS
R528 0_0805_5%
+1.8VS_VCCPLL
VCCPLL1 B6, VCCPLL2 A6, VCCPLL3 A2
330U_D2_2V_Y: C664
10U_0805_6.3V6M: C655
10U_0402_6.3V6K: C654, C653
INTEL Recommend
1*330uF,1*10uF and 2*1uF(0402)
from PDDG 1.0

Sandy Bridge_rPGA_Rev0p61
CONN@

Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

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Title: PROCESSOR(6/7) PWR
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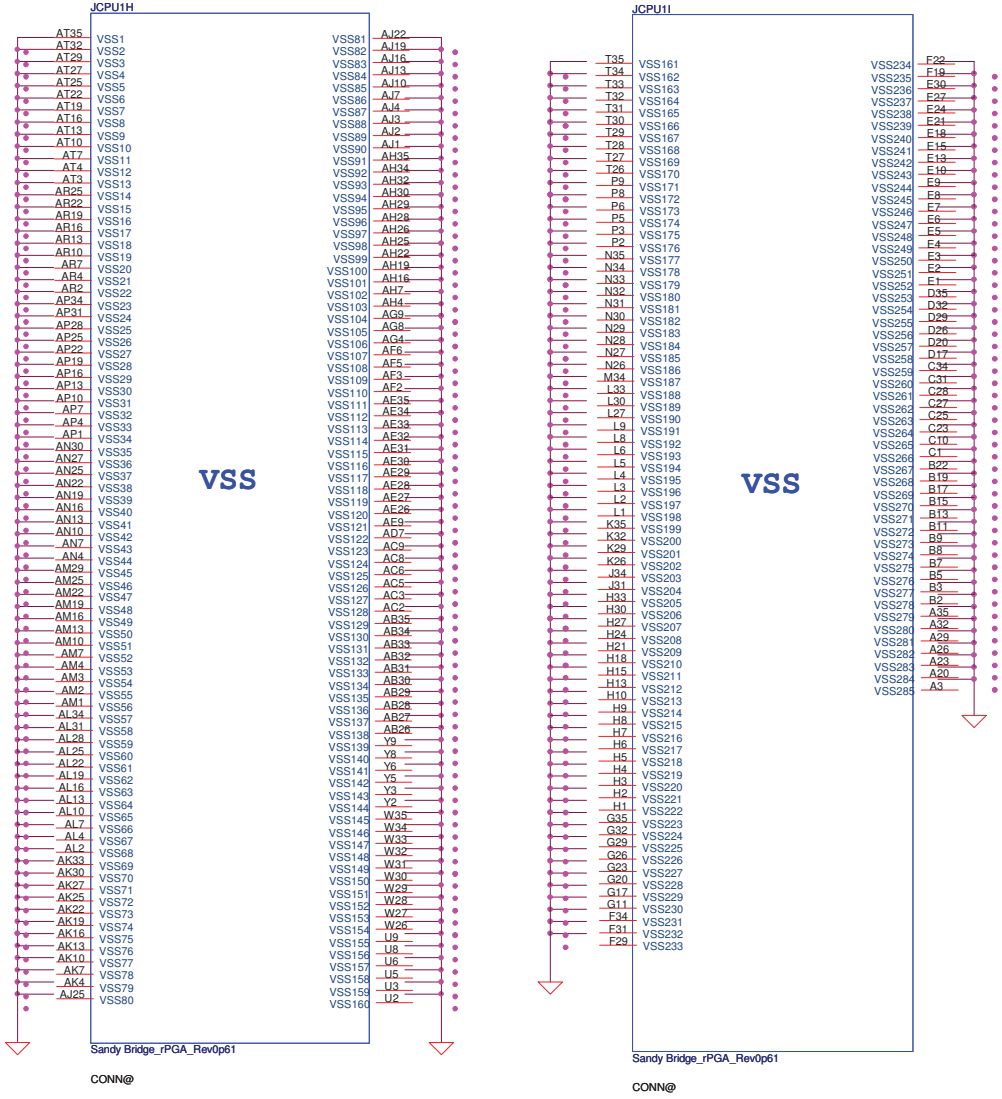

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Issued Date	2010/08/11	Deciphered Date	2011/08/11

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Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
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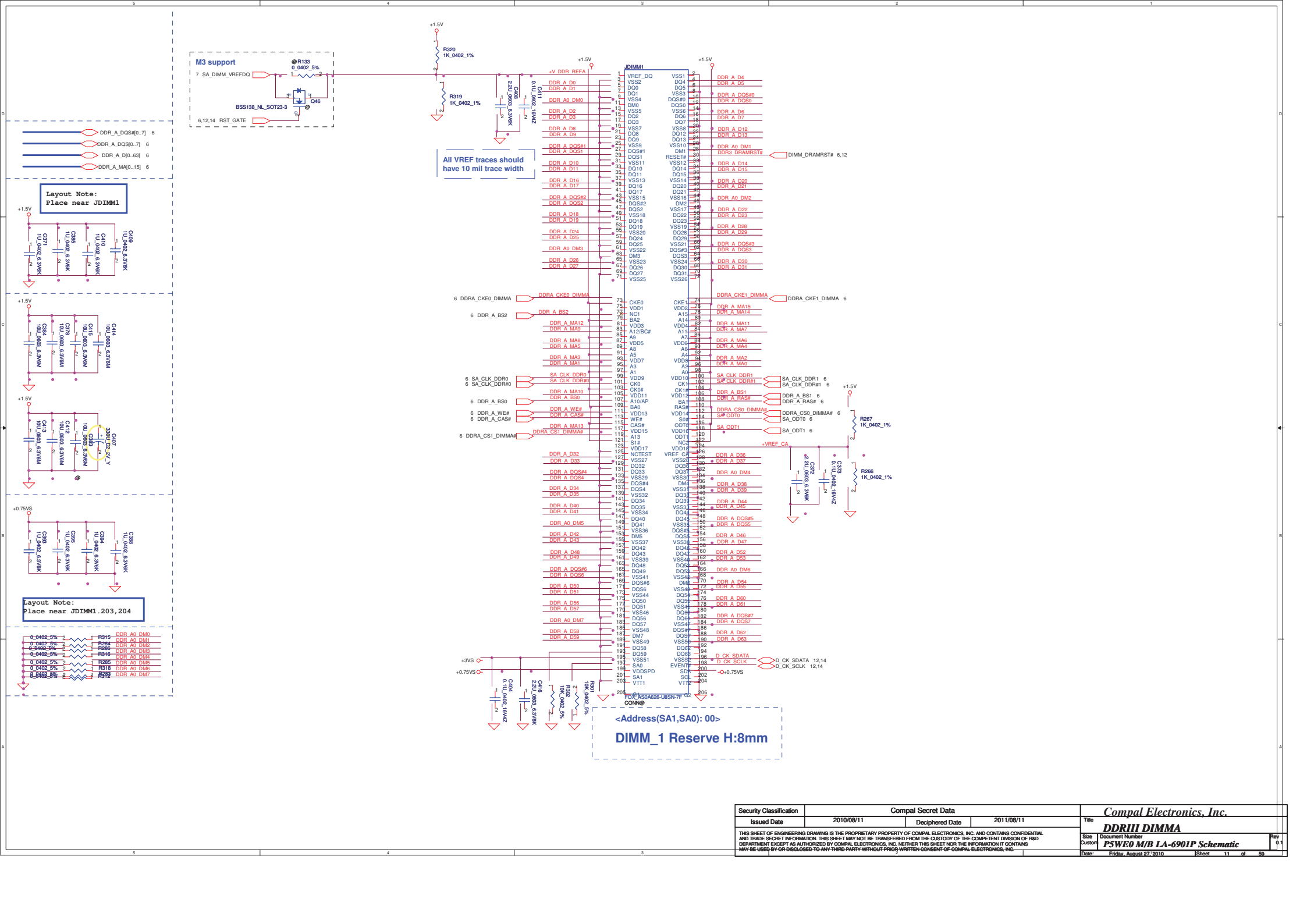

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Issued Date	2010/08/11	Deciphered Date	2011/08/11

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Title: DDRIII DIMMA

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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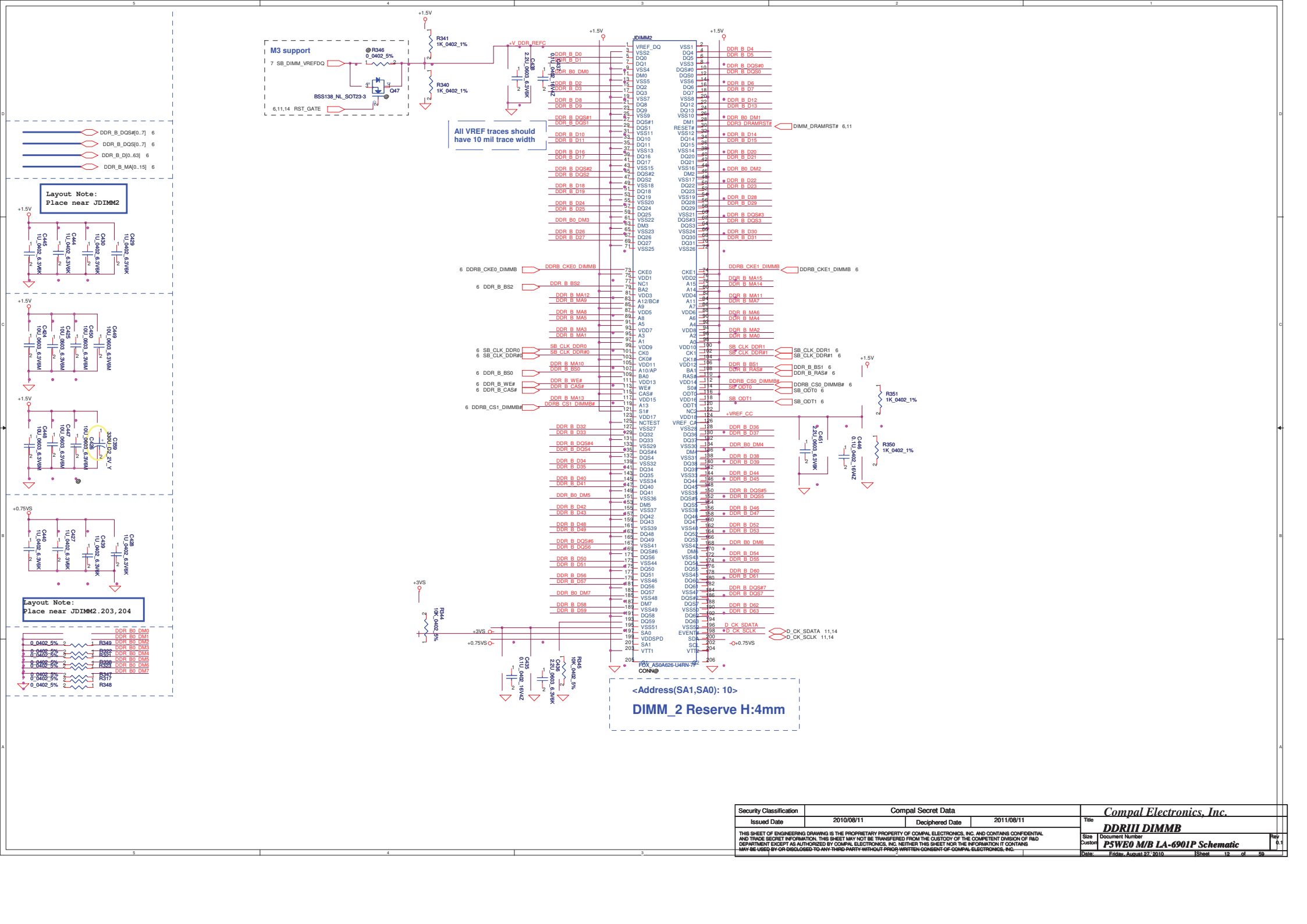

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Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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PCH_RTCX1
PCH_RTCX2
R568 10M_0402_5%
Y3 32.768KHZ_12.5PF_Q13MC14610002
C682 18P_0402_50V8J
C686 18P_0402_50V8J

+RTCVCC
R567 1M_0402_5% SM_INTRUDER#
R585 330K_0402_5% PCH_INTVRMEN

INTVRMEN

* H : Integrated VRM enable
  L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS
R294 @ 1K_0402_5% PCH_SPKR

HIGH= Enable (No Reboot)
* LOW= Disable (Default)

+3VALW_PCH
R556 1K_0402_5%
R557 @ 0_0402_5%
39 HDA_SDO
HDA_SDOUT_PCH

HDA_SDO as Capella ME override (GPIO33)

ME debug mode,this signal has a weak internal PD
* Low = Disabled (Default)
  High = Enabled [Flash Descriptor Security Overide]

+3VALW_PCH
R539 1K_0402_5% HDA_SYNC_PCH

This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
* 1.5V when smapled high
  1.8V when sampled low
  Needs to be pulled High for Huron River platfrom

R544 33_0402_5% 41 HDA_BITCLK_AUDIO HDA_BITCLK_PCH
R542 33_0402_5% 41 HDA_SYNC_AUDIO HDA_SYNC_PCH_R
R545 33_0402_5% 41 HDA_RST_AUDIO# HDA_RST_PCH#
R555 33_0402_5% 41 HDA_SDOUT_AUDIO HDA_SDOUT_PCH

+3VALW_PCH
R666 200_0402_5% PCH_JTAG_TDO
R637 200_0402_5% PCH_JTAG_TMS
R646 200_0402_5% PCH_JTAG_TDI
R671 100_0402_1%
R636 100_0402_1%
R648 100_0402_1%

+RTCBATT
+CHGRTC
R375 1K_0402_5%
+RTCBATT_R
D13 DAN202UT106_SC70-3
20mil
+RTCVCC
20mil
C471 0.1U_0402_16V4Z

RTCRST close RAM door

+RTCVCC
C360 1U_0603_10V6K
R248 20K_0402_5%
R243 20K_0402_5%
C356 1U_0603_10V6K
J7 0_0603_5% @
J8 0_0603_5% @

SRTCRST close RAM door

41 PCH_SPKR
41 HDA_SDIN0

Prevent back drive issue.

+3VS
Q36 BSS138_NL_SOT23-3
R540 @ 0_0402_5%

R674 51_0402_5%

U33A

PCH_RTCX1	A20	RTCX1	RTC
PCH_RTCX2	C20	RTCX2	
PCH_RTCRST#	D20	RTCRST#	
PCH_SRTCRST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	
HDA_BITCLK_PCH	N34	HDA_BCLK	IHDA
HDA_SYNC_PCH	L34	HDA_SYNC	
PCH_SPKR	T10	SPKR	
HDA_RST_PCH#	K34	HDA_RST#	
HDA_SDIN0	E34	HDA_SDIN0	
	G34	HDA_SDIN1	
	C34	HDA_SDIN2	
	A34	HDA_SDIN3	
HDA_SDOUT_PCH	A36	HDA_SDO	
	C36	HDA_DOCK_EN# / GPIO33	
	N32	HDA_DOCK_RST# / GPIO13	
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG
PCH_JTAG_TMS	H7	JTAG_TMS	
PCH_JTAG_TDI	K5	JTAG_TDI	
PCH_JTAG_TDO	H1	JTAG_TDO	
PCH_SPI_CLK	T3	SPI_CLK	SPI
PCH_SPI_CS0#	Y14	SPI_CS0#	
	T1	SPI_CS1#	
PCH_SPI_MOSI	V4	SPI_MOSI	
PCH_SPI_MISO	U3	SPI_MISO	

COUGARPOINT_FCBGA989-D

R681 0_0402_5% PCH_SPI_CLK_1 → PCH_SPI_CLK
R651 0_0402_5% PCH_SPI_CS0#_1 → PCH_SPI_CS0#
R684 0_0402_5% PCH_SPI_MOSI_1 → PCH_SPI_MOSI
R652 0_0402_5% PCH_SPI_MISO_1 → PCH_SPI_MISO

FWH0 / LAD0	C38	LPC_AD0	LPC_AD0 39
FWH1 / LAD1	A38	LPC_AD1	LPC_AD1 39
FWH2 / LAD2	B37	LPC_AD2	LPC_AD2 39
FWH3 / LAD3	C37	LPC_AD3	LPC_AD3 39
FWH4 / LFRAME#	D36	LPC_FRAME#	LPC_FRAME# 39
LDRQ0#	E36		
LDRQ1# / GPIO23	K36		
SERIRQ	V5	SERIRQ	SERIRQ 39
SATA0RXN	AM3	SATA_PRX_DTX_N0	SATA_PRX_DTX_N0 34
SATA0RXP	AM1	SATA_PRX_DTX_P0	SATA_PRX_DTX_P0 34
SATA0TXN	AP7	SATA_PTX_DRX_N0	SATA_PTX_DRX_N0 34
SATA0TXP	AP5		HDD
SATA1RXN	AM10		
SATA1RXP	AM8		
SATA1TXN	AP11		
SATA1TXP	AP10		
SATA2RXN	AD7	SATA_PRX_DTX_N2	SATA_PRX_DTX_N2 34
SATA2RXP	AD5	SATA_PRX_DTX_P2	SATA_PRX_DTX_P2 34
SATA2TXN	AH5	SATA_PTX_DRX_N2	SATA_PTX_DRX_N2 34
SATA2TXP	AH4		ODD
SATA3RXN	AB8		
SATA3RXP	AB10		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	Y7		
SATA4RXP	Y5		
SATA4TXN	AD3		
SATA4TXP	AD1		
SATA5RXN	Y3		
SATA5RXP	Y1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	Y11	SATA_COMP	R260 37.4_0402_1% +1.05VS_PCH
SATAICOMPI	Y10		
SATA3RCOMPO	AB12	SATA3_COMP	R241 49.9_0402_1% +1.05VS_PCH
SATA3COMPI	AB13		
SATA3RBIAS	AH1	RBIAS_SATA3	R625 750_0402_1%
SATALED#	P3	PCH_SATALED#	PCH_SATALED# 40
SATA0GP / GPIO21	V14	SGEN#	
SATA1GP / GPIO19	P1	PCH_GPIO19	R655 +3VALW_PCH

GPIO19 has internal PU

+3VS
R654 3.3K_0402_5% PCH_SPI_CS0#_1 → SPI_WP1#
R667 3.3K_0402_5% SPI_HOLD1#

U36
CS# VCC
WP# SCLK
HOLD# SI
GND SO
MX25L3205DM2I-12G SOP 8P
SA000021M00

PCH_SPI_CLK_1
PCH_SPI_MOSI_1
PCH_SPI_MISO_1

SPI ROM 4MB (4MB)
Footprint 200mil

+RTCBATT
JBATT1
CONN@ SUYIN_060003HA002G202ZL
20100416_add

SERIRQ R275 10K_0402_5%
PCH_SATALED# R640 10K_0402_5%
PCH_GPIO19 R624 10K_0402_5%
+3VS

+3VS
SGEN#
R259 10K_0402_5%
R258 @ 10K_0402_5%

	GPIO21 SGEN#
Switchable GPU	0
*Non-Switchable	1

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
* SPI	1	1

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 13 of 59

PCIE LAN
Mini Card 1
Mini Card 2
USB3.0 Right
USB3.0 Left
USB3.0
Controller Link
SMBUS
PCI-E*
CLOCKS
FLEX CLOCKS
U33B
COUGARPOINT_FCBGA989~D
<BOM Structure>
For DDR
Pull up at EC side.
For VGA,EC
Pull down 10K ohm
for using internal Clock
Pull high @ VGA side
for safe
Reserve for EMI please close to UH4

	GPIO67 DGPU_PRSNT#
DIS,OPTIMUS	0
UMA	1

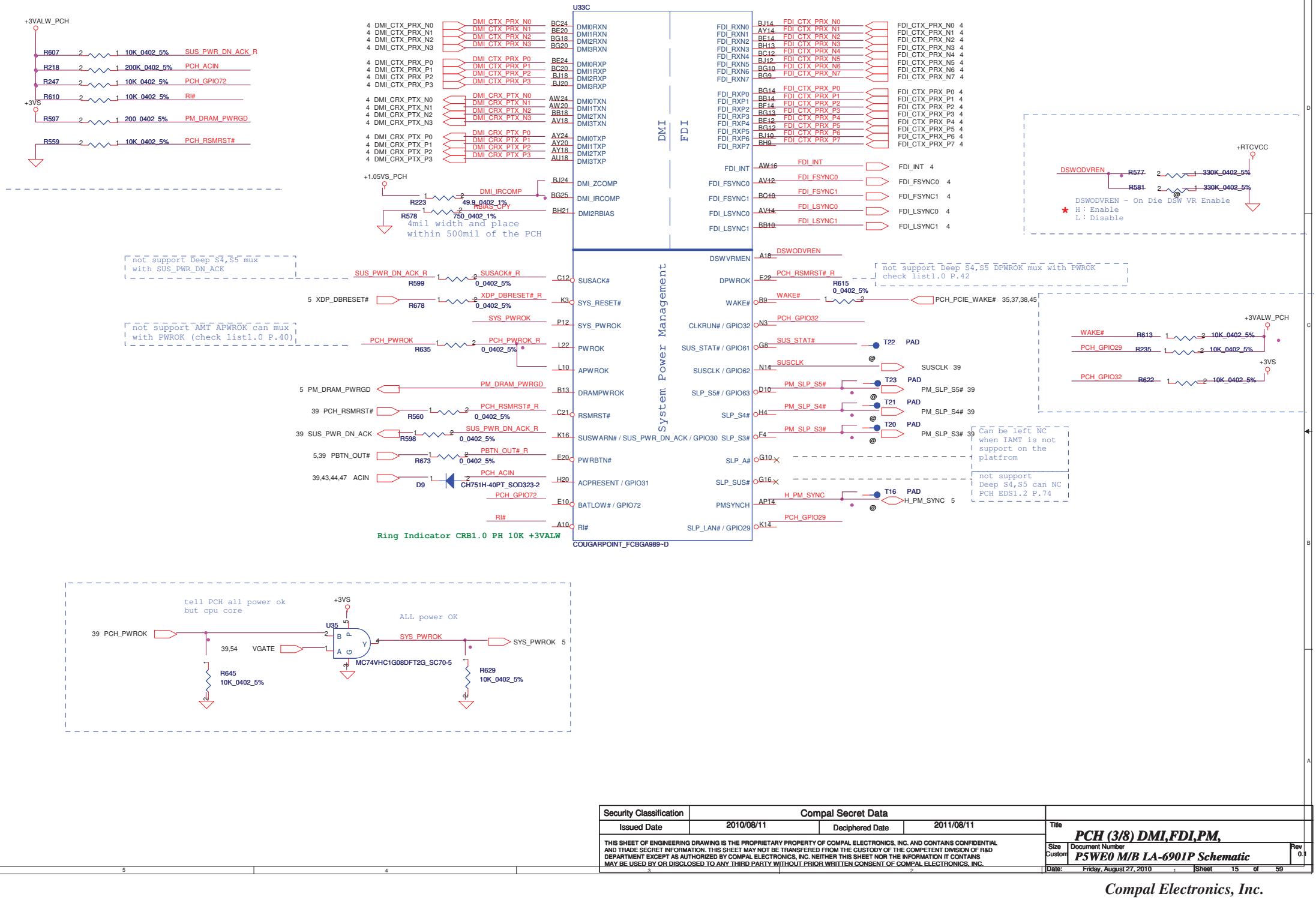
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 14 of 59



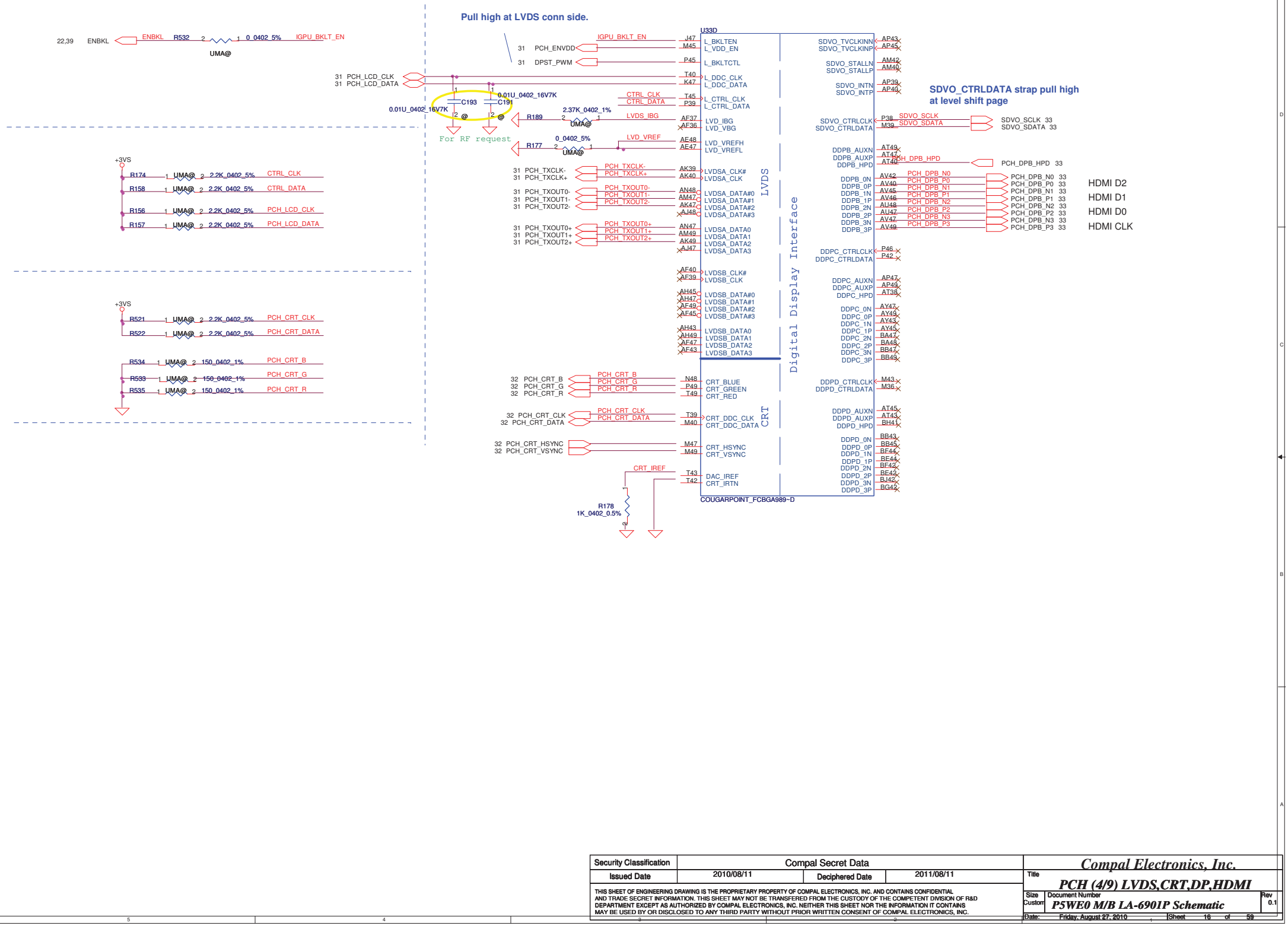
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Title: **PCH (3/8) DMI,FDI,PM,**

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 15 of 59

Compal Electronics, Inc.



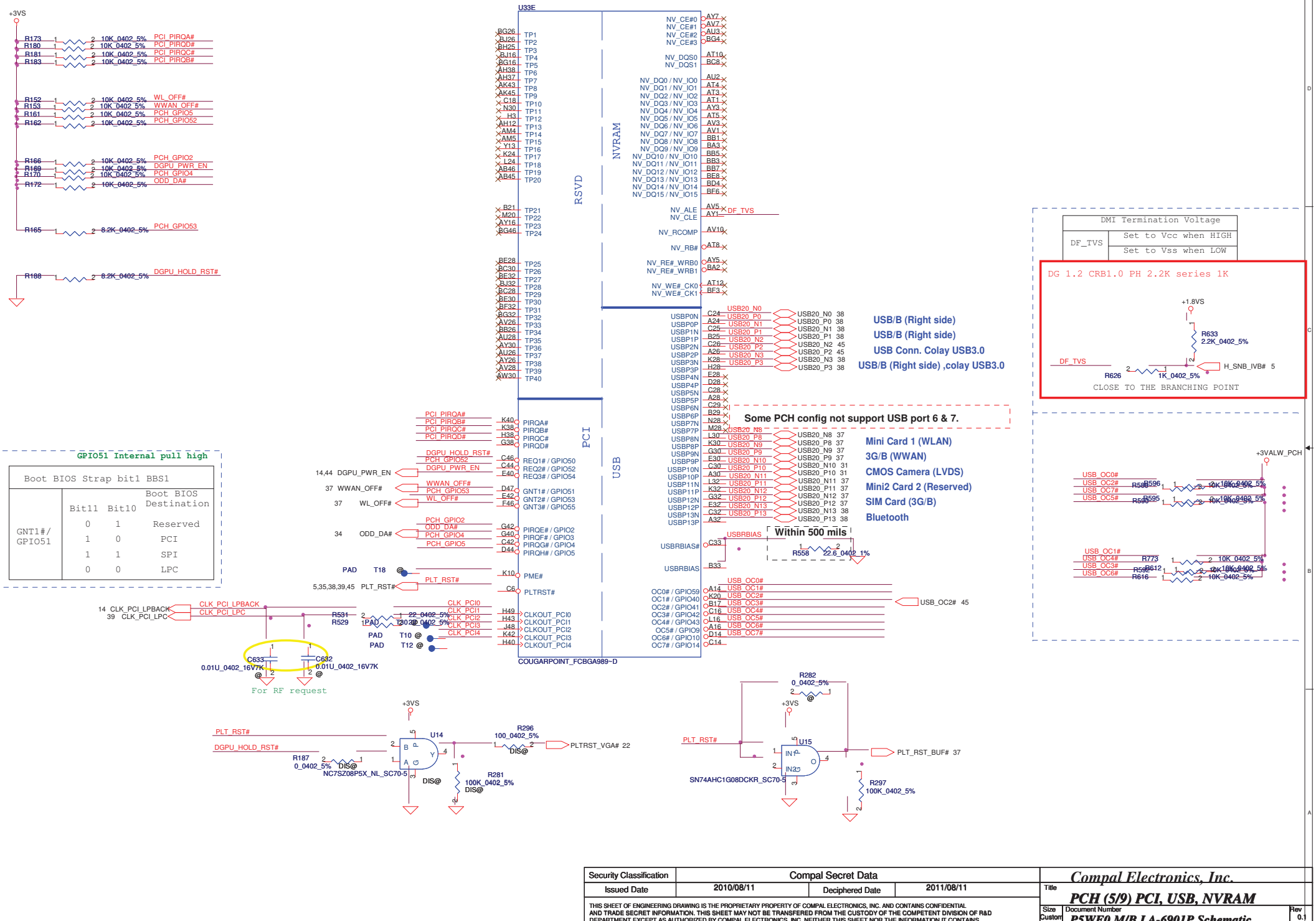
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 16 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 17 of 59

HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+3VALW_PCH — R272 1K_0402_5% — PCH_GPIO28
+3VALW_PCH — R768 4.7K_0402_5%

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R661 10K_0402_5% — PCH_GPIO27

+3VS
R623 1K_0402_5% NOPT@ — OPTIMUS_EN#
R639 100K_0402_5% OPT@

	GPIO38 OPTIMUS_EN#
★ OPTIMUS	0
Non-OPTIMUS	1

+3VS
R277 100K_0402_5% — PCH_GPIO37
R276 10K_0402_5% — PCH_GPIO0
R546 10K_0402_5% — PCH_GPIO1
R191 10K_0402_5% — DGPU_HPD_INT#
R641 10K_0402_5% — PCH_GPIO16
R194 10K_0402_5% — DGPU_PWROK
R290 10K_0402_5% — PCH_GPIO22
R649 10K_0402_5% — PCH_GPIO39
R291 100K_0402_5% — ODD_DETECT#
R619 10K_0402_5% — BT_ON#
R292 10K_0402_5% — PCH_GPIO48
R274 10K_0402_5% — PCH_GPIO49

+3VALW_PCH
R262 10K_0402_5% — PCH_GPIO24
R620 10K_0402_5% — PCH_GPIO12
R672 1K_0402_5% — SMIB
R263 10K_0402_5% — PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

U33F

PCH_GPIO0	T7	BMBUSY# / GPIO0	
PCH_GPIO1	A42	TACH1 / GPIO1	
33 DGPU_HPD_INT#	H36	TACH2 / GPIO6	
39 EC_SCI#	E38	TACH3 / GPIO7	
39 EC_SMI#	C10	GPIO8	
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12	
38,45 SMIB	G2	GPIO15	
PCH_GPIO16	U2	SATA4GP / GPIO16	
53 VGA_PWROK — R193 0_0402_5% — DGPU_PWROK	D40	TACH0 / GPIO17	
PCH_GPIO22	T5	SCLOCK / GPIO22	
PCH_GPIO24	E8	GPIO24 / MEM_LED	
PCH_GPIO27	E16	GPIO27	
PCH_GPIO28	P8	GPIO28	
37,38 BT_ON#	K1	STP_PCI# / GPIO34	
	K4	GPIO35	
34 ODD_DETECT#	V8	SATA2GP / GPIO36	
PCH_GPIO37	M5	SATA3GP / GPIO37	
OPTIMUS_EN#	N2	SLOAD / GPIO38	
PCH_GPIO39	M3	SDATAOUT0 / GPIO39	
PCH_GPIO48	V13	SDATAOUT1 / GPIO48	
PCH_GPIO49	V3	SATA5GP / GPIO49	
PCH_GPIO57	D6	GPIO57	

GPIO

	C40	TACH4 / GPIO68	ODD_EN# — ODD_EN# 34
	B41	TACH5 / GPIO69	PCH_GPIO69
	C41	TACH6 / GPIO70	PCH_GPIO70
	A40	TACH7 / GPIO71	PCH_GPIO71
	P4	A20GATE	GATEA20 39
	AU16	PECI	PCH_PECI_R — 0_0402_5%@R239 — H_PECI 5,39
	P5	RCIN#	EC_KBRST# — EC_KBRST# 39
	AY11	PROCPWRGD	H_CPUPWRGD 5
	AY10	THRMTRIP#	PCH_THRMTRIP#_R — R627 390_0402_5% — H_THRMTRIP# — H_THRMTRIP# 5
	T14	INIT3_3V	
	AH8	NC_1	
	AK11	NC_2	
	AH10	NC_3	
	AK10	NC_4	
	P37	NC_5	

CPU/MISC

INIT3_3V Checklist1.0 P.59
This signal has weak internal PU, can't pull low,leave NC

TS_VSS1~4
PD to GND

+3VS
R278 10K_0402_5%

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130 degree shut sown

+3VS
ODD_EN# — R771 10K_0402_5%
EC_KBRST# — R279 10K_0402_5%

PAD T61	A4	VSS_NCTF_1	BG2 T58 PAD
PAD T46	A44	VSS_NCTF_2	BG48 T39 PAD
PAD T44	A45	VSS_NCTF_3	BH3 T59 PAD
PAD T41	A46	VSS_NCTF_4	BH47 T40 PAD
PAD T52	A5	VSS_NCTF_5	BJ4 T60 PAD
PAD T51	A6	VSS_NCTF_6	BJ44 T45 PAD
PAD T64	B3	VSS_NCTF_7	BJ45 T43 PAD
PAD T37	B47	VSS_NCTF_8	BJ46 T42 PAD
PAD T55	BD1	VSS_NCTF_9	BJ5 T50 PAD
PAD T34	BD49	VSS_NCTF_10	BJ6 T49 PAD
PAD T56	BE1	VSS_NCTF_11	C2 T65 PAD
PAD T35	BE49	VSS_NCTF_12	C48 T38 PAD
PAD T57	BF1	VSS_NCTF_13	D1 T63 PAD
PAD T36	BF49	VSS_NCTF_14	D49 T32 PAD
		VSS_NCTF_15	E1 T54 PAD
		VSS_NCTF_16	F49 T33 PAD
		VSS_NCTF_17	F1 T53 PAD
		VSS_NCTF_18	F49 T31 PAD
		VSS_NCTF_19	
		VSS_NCTF_20	
		VSS_NCTF_21	
		VSS_NCTF_22	
		VSS_NCTF_23	
		VSS_NCTF_24	
		VSS_NCTF_25	
		VSS_NCTF_26	
		VSS_NCTF_27	
		VSS_NCTF_28	
		VSS_NCTF_29	
		VSS_NCTF_30	
		VSS_NCTF_31	
		VSS_NCTF_32	

NCTF

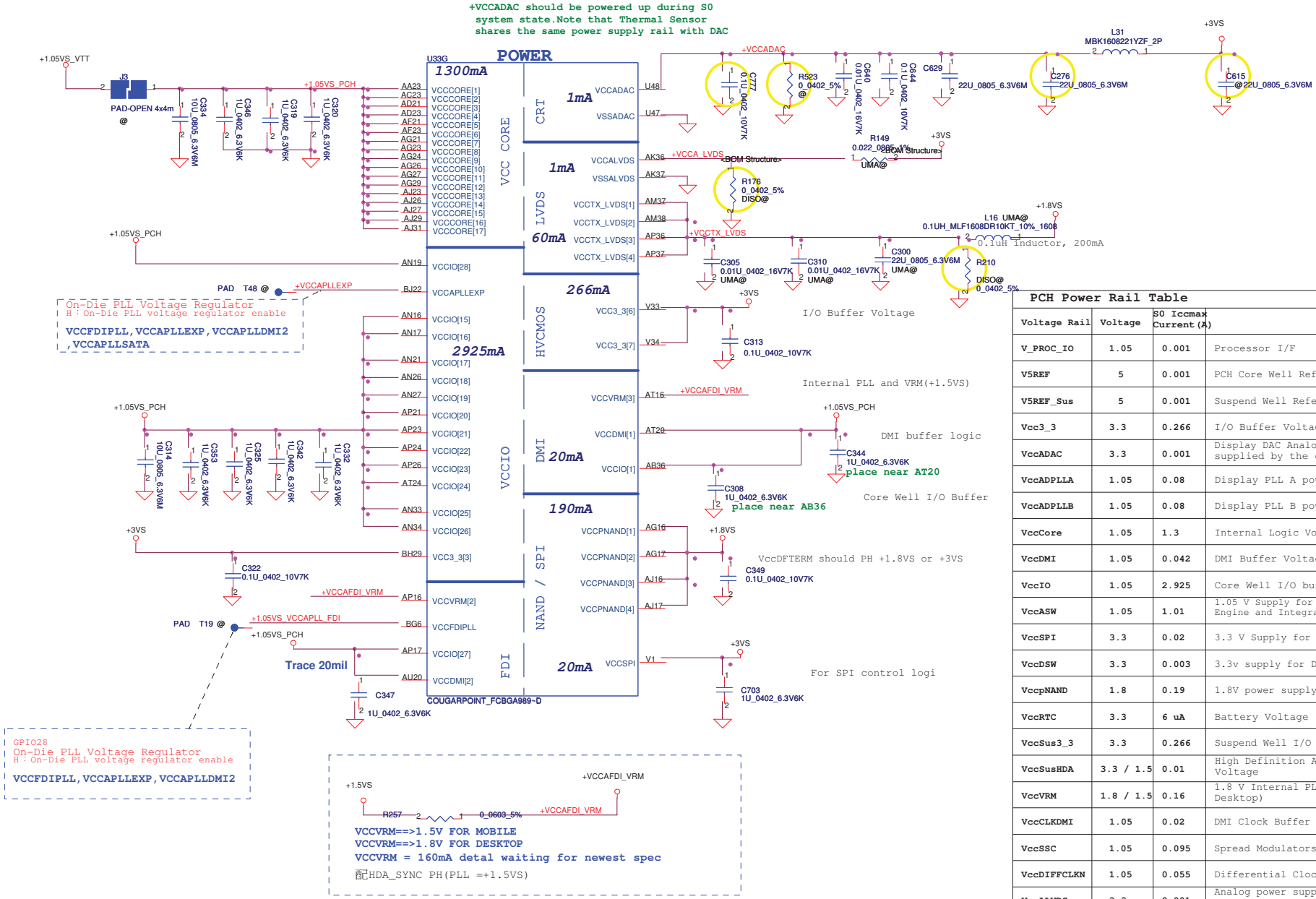
COUGARPOINT_FCBGA989~D
<BOM Structure>

+3VS
R554 10K_0402_5% — PCH_GPIO69
R548 10K_0402_5% — PCH_GPIO70
R550 10K_0402_5% — PCH_GPIO71
R553 10K_0402_5%
R549 10K_0402_5%
R551 10K_0402_5%

Project ID	GPIO69	GPIO70	GPIO71
★ P5WE0	0	0	0
P7YE0	0	0	0
x	0	1	0
x	0	1	1
x	1	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.
Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1
Date: Friday, August 27, 2010 | Sheet 18 of 59



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

U33J

+3VS
R150 0_0805_5%
L14 10UH_LB2012T100MR_20%
+3VS_VCC_CLKF33
C277 10U_0805_10V4Z
C304 1U_0402_6.3V6K

+1.05V analog internal clock PLL Can NC
+1.05VS_PCH
R167 0_0603_5%
+VCCACLK
AD49 VCCACLK

Not support Deep S4,S5 connect to +3VALW
+3VALW_PCH
C340 0.1U_0402_10V7K
T16 VCCDSW3_3

PAD T17 @ +PCH_VCCDSW
V12 DCPSUSBYP

3mA

+3VS_VCC_CLKF33
T38 VCC3_3[5]

suppied by internal 1.05V VR must NC
PAD T11 @ +VCCAPLL_CPY_PCH
BH23 VCCAPLLDMI2

119mA

USB

+1.05VS_PCH
AL29 VCCIO[14]

PAD T13 @ +VCCSUS1
AL24 DCPSUS[3]

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

+1.05VS_PCH
L12 10UH_LB2012T100MR_20%
+1.05VS_VCCA_A_DPL
C279 220U_B2_2.5VM_R35
C286 1U_0402_6.3V6K
L11 10UH_LB2012T100MR_20%
+1.05VS_VCCA_B_DPL
C278 220U_B2_2.5VM_R35
C285 1U_0402_6.3V6K
SGA00001700
220U 2.5V M B2
ESR 35mohm@100Khz

+1.05VS_PCH
C336 22U_0805_6.3V6M
C335 22U_0805_6.3V6M
C326 1U_0402_6.3V6K
C327 1U_0402_6.3V6K
C316 1U_0402_6.3V6K

AA19 VCCASW[1]
AA21 VCCASW[2]
AA24 VCCASW[3]
AA26 VCCASW[4]
AA27 VCCASW[5]
AA29 VCCASW[6]
AA31 VCCASW[7]
AC26 VCCASW[8]
AC27 VCCASW[9]
AC29 VCCASW[10]
AC31 VCCASW[11]
AD29 VCCASW[12]
AD31 VCCASW[13]
W21 VCCASW[14]
W23 VCCASW[15]
W24 VCCASW[16]
W26 VCCASW[17]
W29 VCCASW[18]
W31 VCCASW[19]
W33 VCCASW[20]

1010mA

Clock and Miscellaneous

+VCCRTCEXT
N16 DCPRTC

C348 0.1U_0402_10V7K
+VCCAFDI_VRM
Y49 VCCVRM[4]

+1.05VS_VCCA_A_DPL
BD47 VCCADPLLA
+1.05VS_VCCA_B_DPL
BF47 VCCADPLLB

80mA
80mA

SATA

+1.05VS_PCH
C311 1U_0402_6.3V6K Place near AF17
C312 1U_0402_6.3V6K Place near AG33
C317 1U_0402_6.3V6K Place near AF33, AF34,AG34

AF17 VCCIO[7]
AF33 VCCIO[8]
AF34 VCCIO[9]
AG34 VCCIO[11]

55mA

AG33 VCCIO[10]

95mA

+VCCSST
C354 0.1U_0402_10V7K
V16 DCPSST

+1.05VM_VCCSUS
T17 DCPSUS[1]
V19 DCPSUS[2]

supplied by internal 1.05V VR Must NC
PAD T15 @

1mA

CPU

+1.05VS_PCH
C700 4.7U_0603_6.3V6K
C684 0.1U_0402_10V7K
C693 0.1U_0402_10V7K
Place near BJ8
BJ8 V_PROC_IO

MISC

+RTCVCC
C331 1U_0402_6.3V6K
C685 0.1U_0402_10V7K
C687 0.1U_0402_10V7K
A22 VCCRTC

RTC

10mA

VCCSUSHDA

COUGARPOINT_FCBGA989~D

VCCIO[29] N26
VCCIO[30] P26
VCCIO[31] P28
VCCIO[32] T27
VCCIO[33] T29
+1.05VS_PCH
C321 1U_0402_6.3V6K

VCCSUS3_3[7] T23
VCCSUS3_3[8] T24
VCCSUS3_3[9] V23
VCCSUS3_3[10] V24
VCCSUS3_3[6] P24
+3VALW_PCH
C330 0.1U_0402_10V7K Place near T24
C333 0.1U_0402_10V7K Place near T24

VCCIO[34] T26
+1.05VS_PCH

1mA
V5REF_SUS M26
+PCH_V5REF_SUS

DCPSUS[4] AN23
+VCCA_USBSUS
+3VALW_PCH
@ T14 PAD
supplied by internal 1.05V VR Must NC
VCCSUS3_3[1] AN24

1mA
V5REF P34
+PCH_V5REF_RUN

PCI/GPIO/LPC

VCCSUS3_3[2] N20
VCCSUS3_3[3] N22
VCCSUS3_3[4] P20
VCCSUS3_3[5] P22
+3V_VCCPSUS
+3VALW_PCH
C352 1U_0402_6.3V6K

VCC3_3[1] AA16
VCC3_3[8] W16
VCC3_3[4] T34
+3VS
C704 0.1U_0402_10V7K Place near J2
C343 0.1U_0402_10V7K Place near A16,W16
C309 0.1U_0402_10V7K Place near T24

VCC3_3[2] AJ2
+1.05VS_PCH

VCCIO[5] AF13
VCCIO[12] AH13
VCCIO[13] AH14
VCCIO[6] AF14
VCCAPLLSATA AK1
+VCCSATAPLL
@ T62 PAD
<BOM Structure>
C350 1U_0402_6.3V6K

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

VCCVRM[1] AF11
+VCCAFDI_VRM
+VCCAFDI_VRM

VCCIO[2] AC16
VCCIO[3] AC17
VCCIO[4] AD17
+1.05VS_PCH
C351 1U_0402_6.3V6K

VCCASW[22] T21
VCCASW[23] V21
VCCASW[21] T19
+VCCME_22
+VCCME_23
+VCCME_21
R237 0_0603_5%
R224 0_0603_5%
R236 0_0603_5%
+1.05VS_PCH

VCCSUSHDA P32
+VCCSUSHDA
R206 0_0603_5%
+3VALW_PCH
Need +3VALW and 0.1U close PCH
C315 0.1U_0402_16V4Z

+5VALW_PCH
+3VALW_PCH
R202 100_0402_5%
D8 CH751H-40PT_SOD323-2
+PCH_V5REF_SUS
C318 0.1U_0603_25V7K

+5VS
+3VS
R148 100_0402_5%
D7 CH751H-40PT_SOD323-2
+PCH_V5REF_RUN
C244 1U_0603_10V6K

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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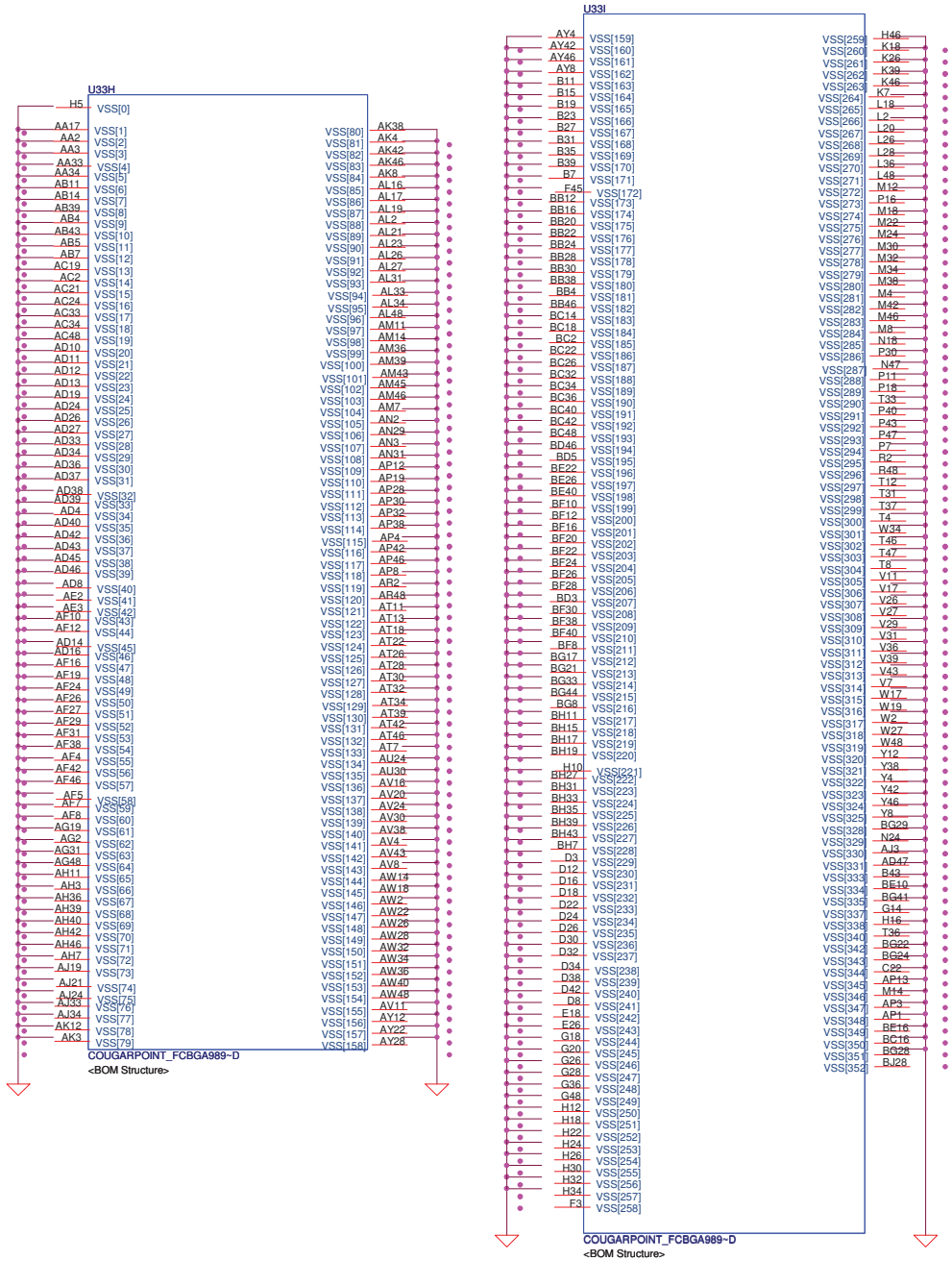

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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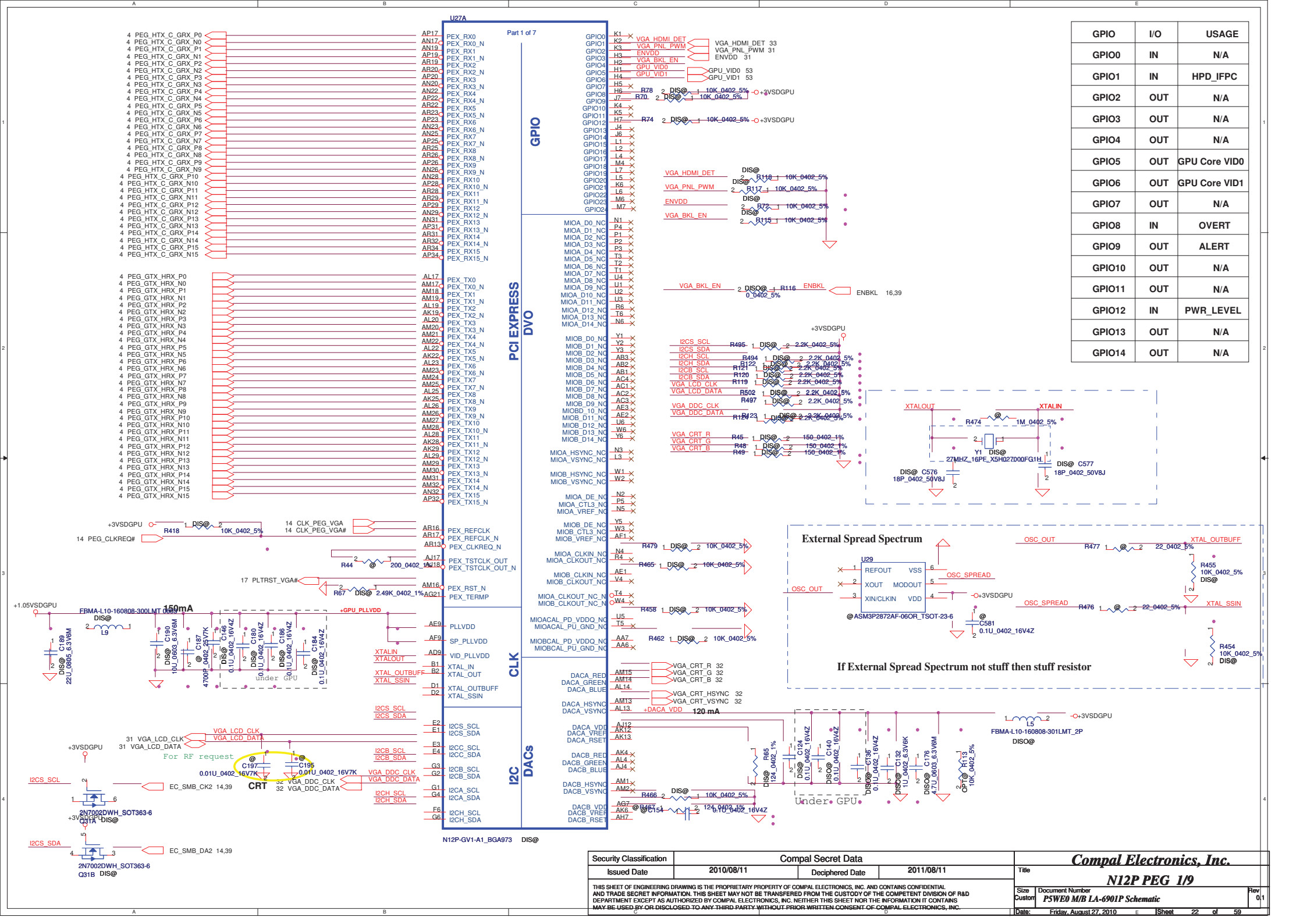

GPIO	I/O	USAGE
GPIO0	IN	N/A
GPIO1	IN	HPD_IFPC
GPIO2	OUT	N/A
GPIO3	OUT	N/A
GPIO4	OUT	N/A
GPIO5	OUT	GPU Core VID0
GPIO6	OUT	GPU Core VID1
GPIO7	OUT	N/A
GPIO8	IN	OVERT
GPIO9	OUT	ALERT
GPIO10	OUT	N/A
GPIO11	OUT	N/A
GPIO12	IN	PWR_LEVEL
GPIO13	OUT	N/A
GPIO14	OUT	N/A

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: N12P PEG 1/9

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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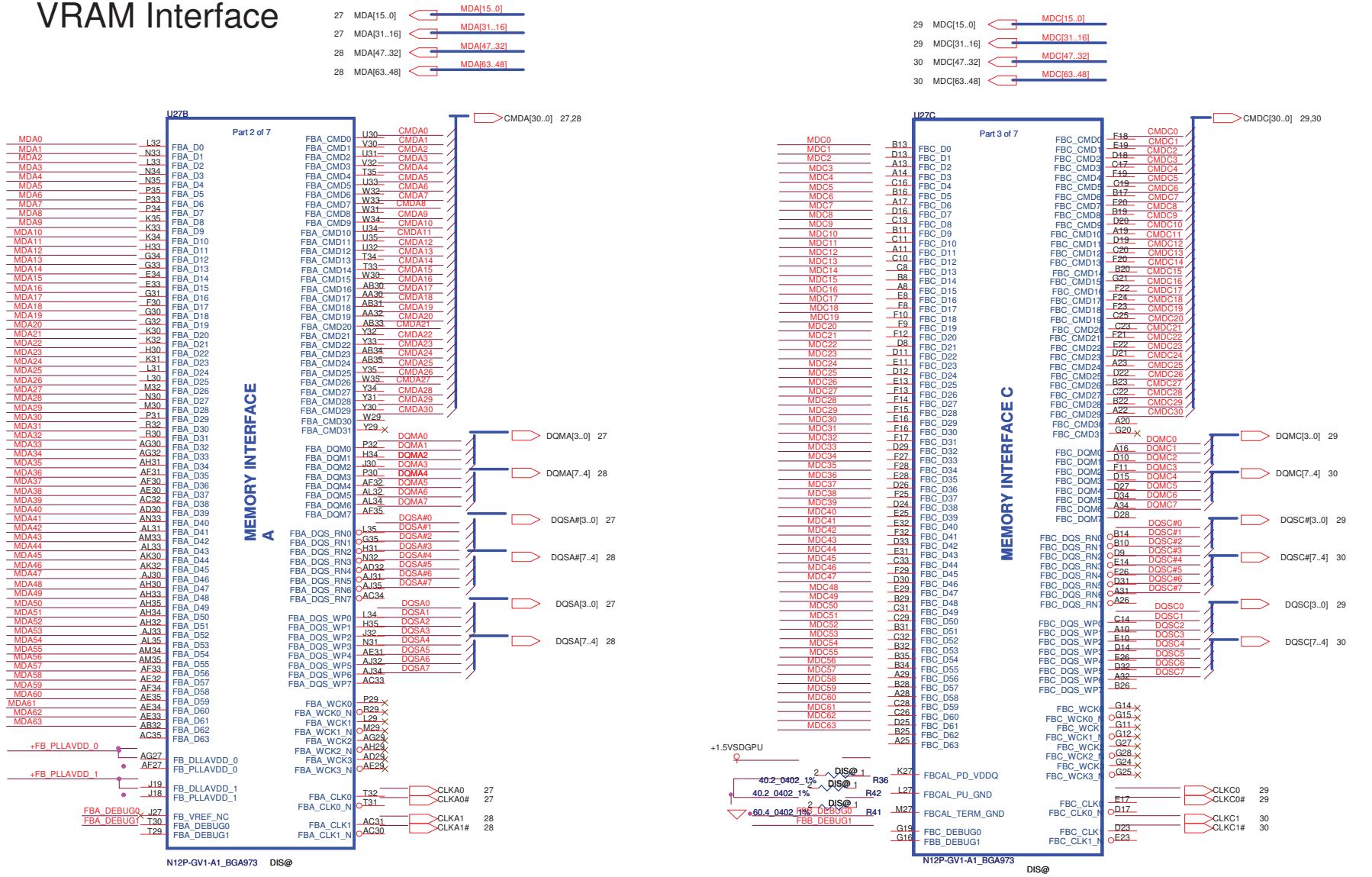
VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: N12P VRAM 2/9

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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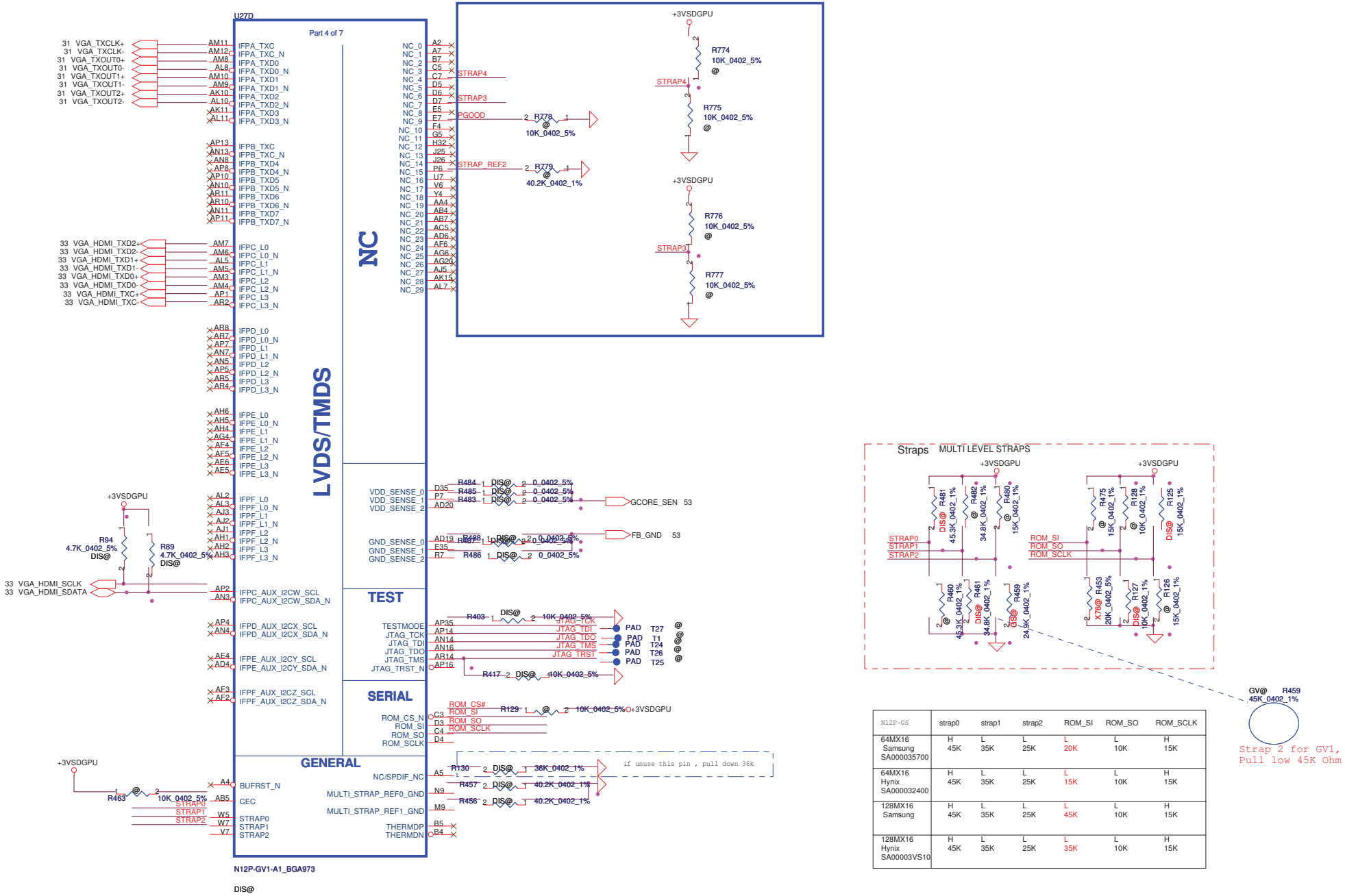
For GB2-128 & GB2b-128 colayout....



GV@ R459 45K_0402_1%

Strap 2 for GV1, Pull low 45K Ohm

N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
128MX16 Samsung	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

Compal Electronics, Inc.

Title: N12P LVDS 3/9

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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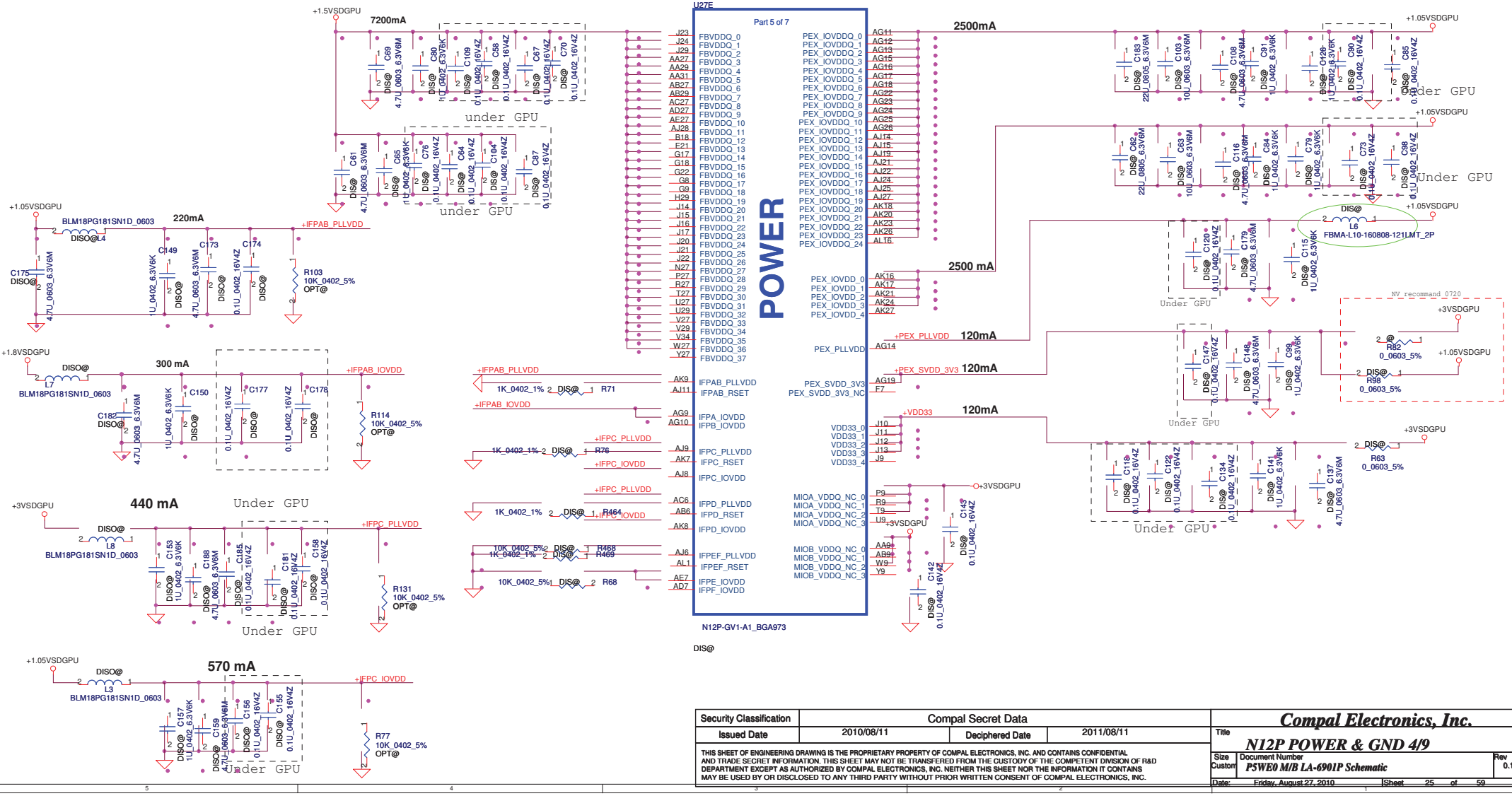

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: **N12P POWER & GND 4/9**

Size	Document Number	Rev
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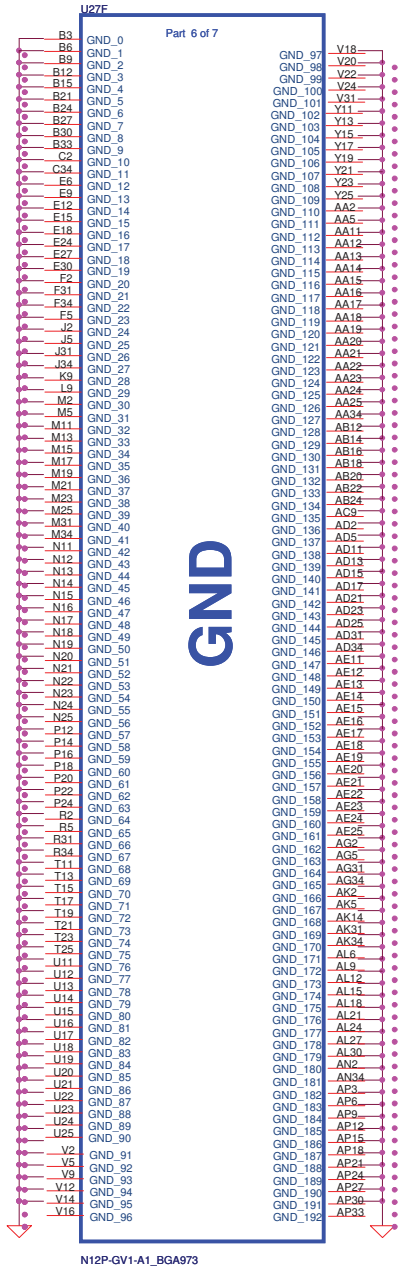
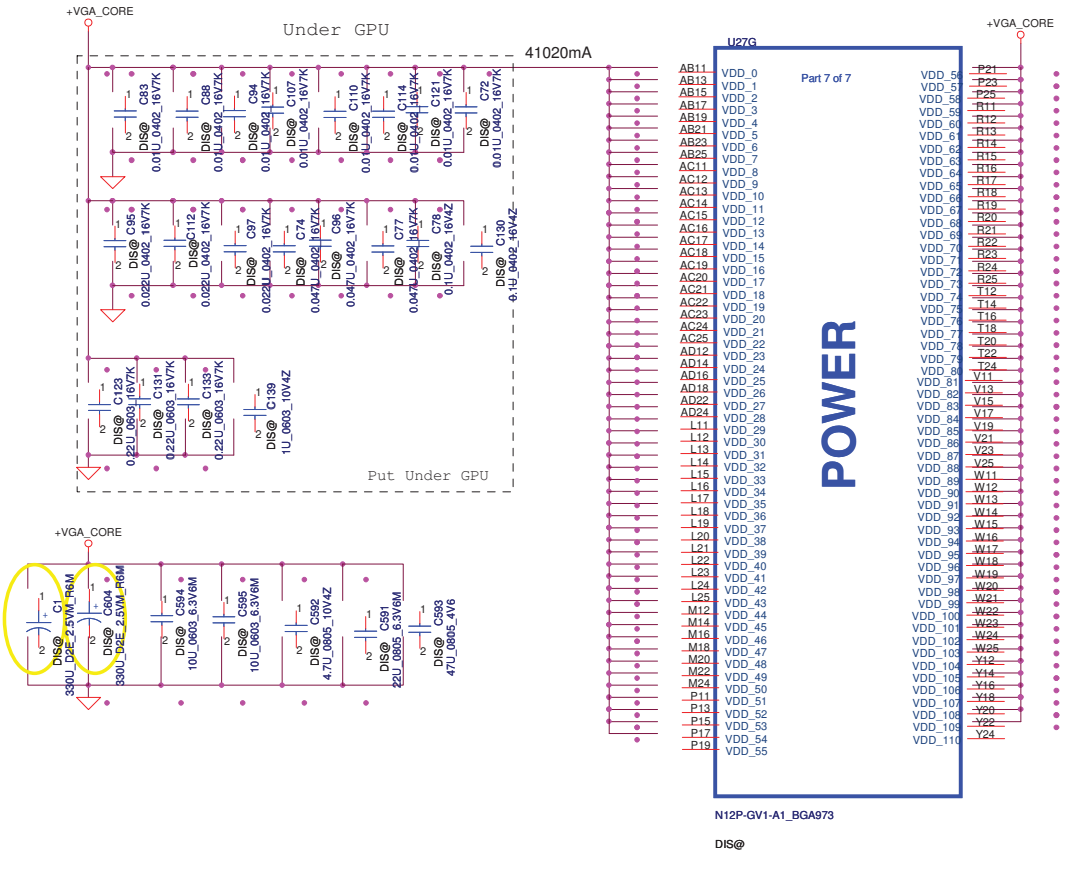




Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

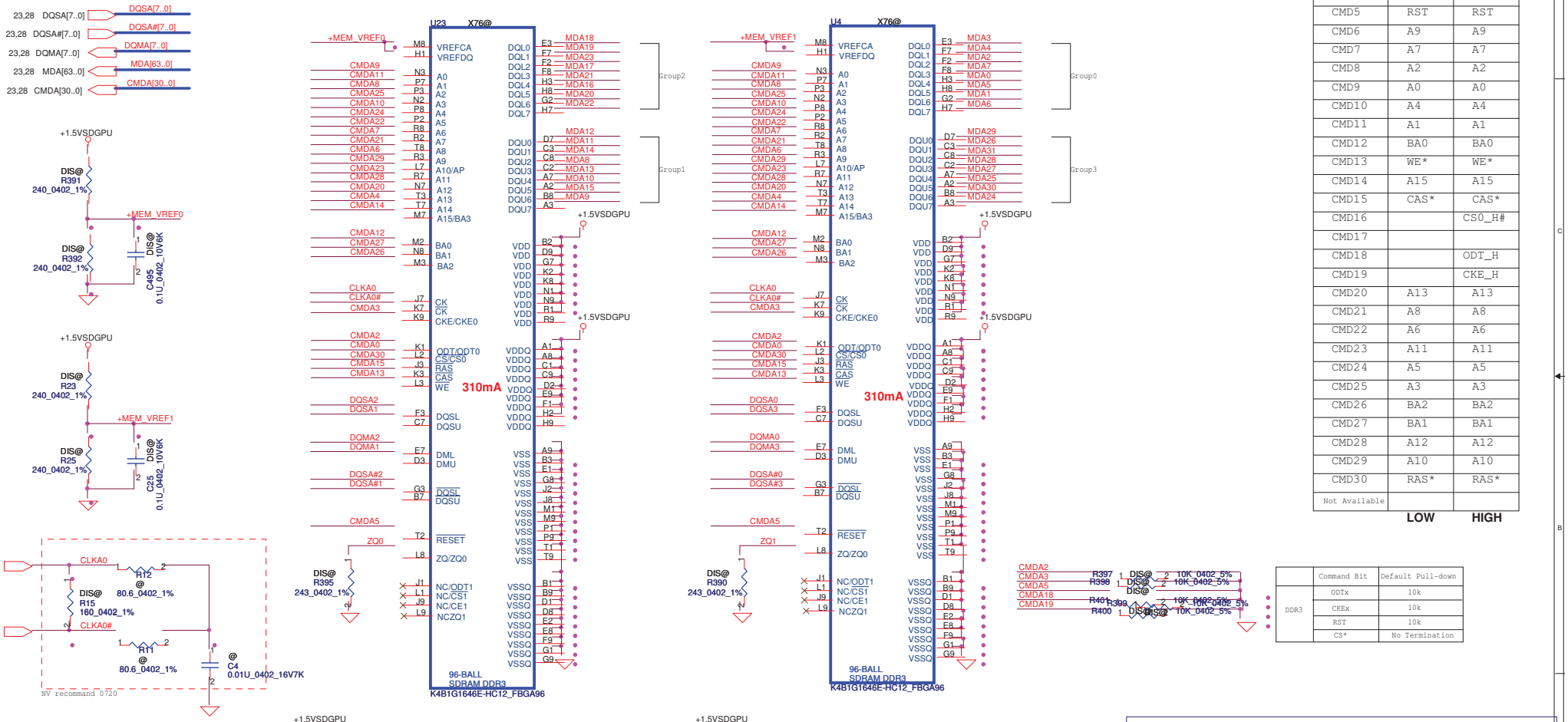
Title: N12P POWER & GND 5/9

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 26 of 59

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: N12P DDR3 6/9

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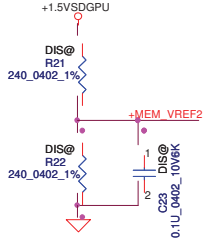
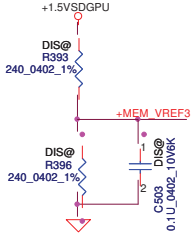
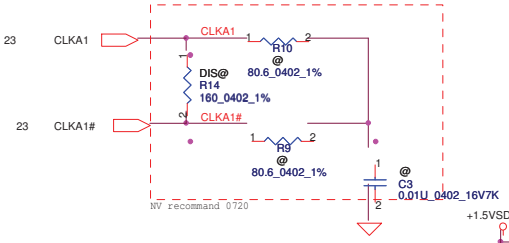
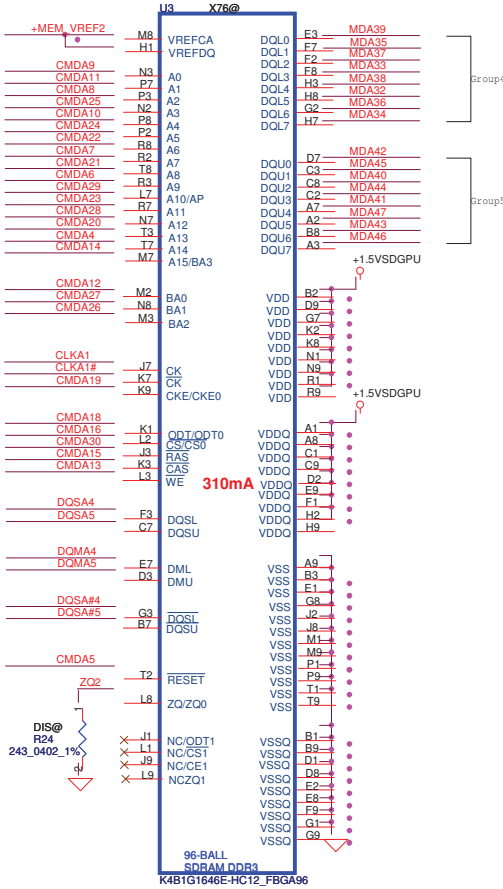
VRAM DDR3 chips (1GB)

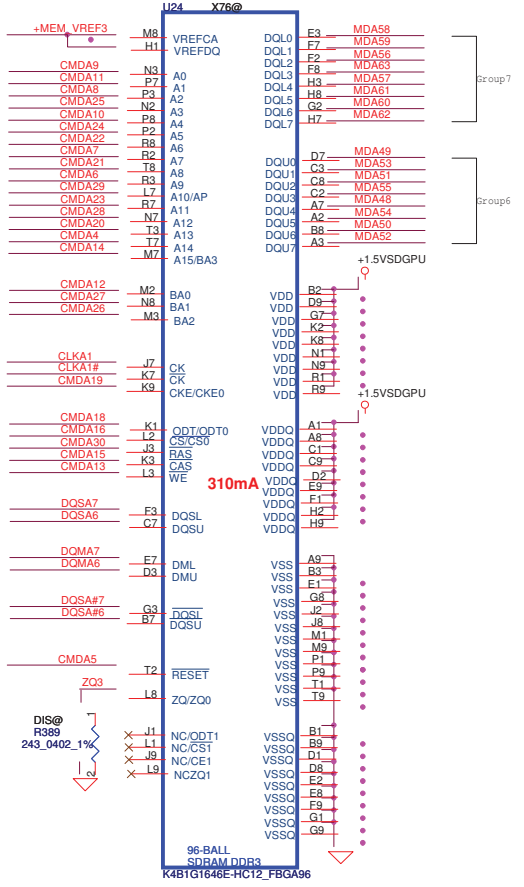
64Mx16 DDR3 *8==>1GB

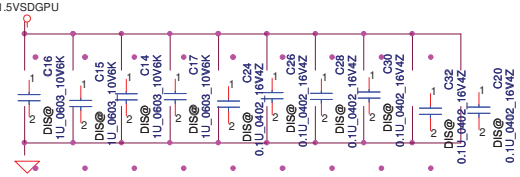


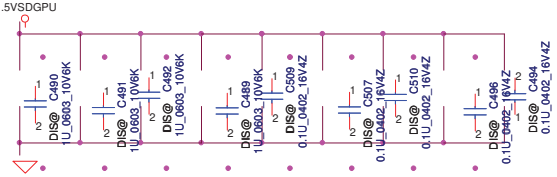












Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.			
Title: N12P DDR3 7/9			
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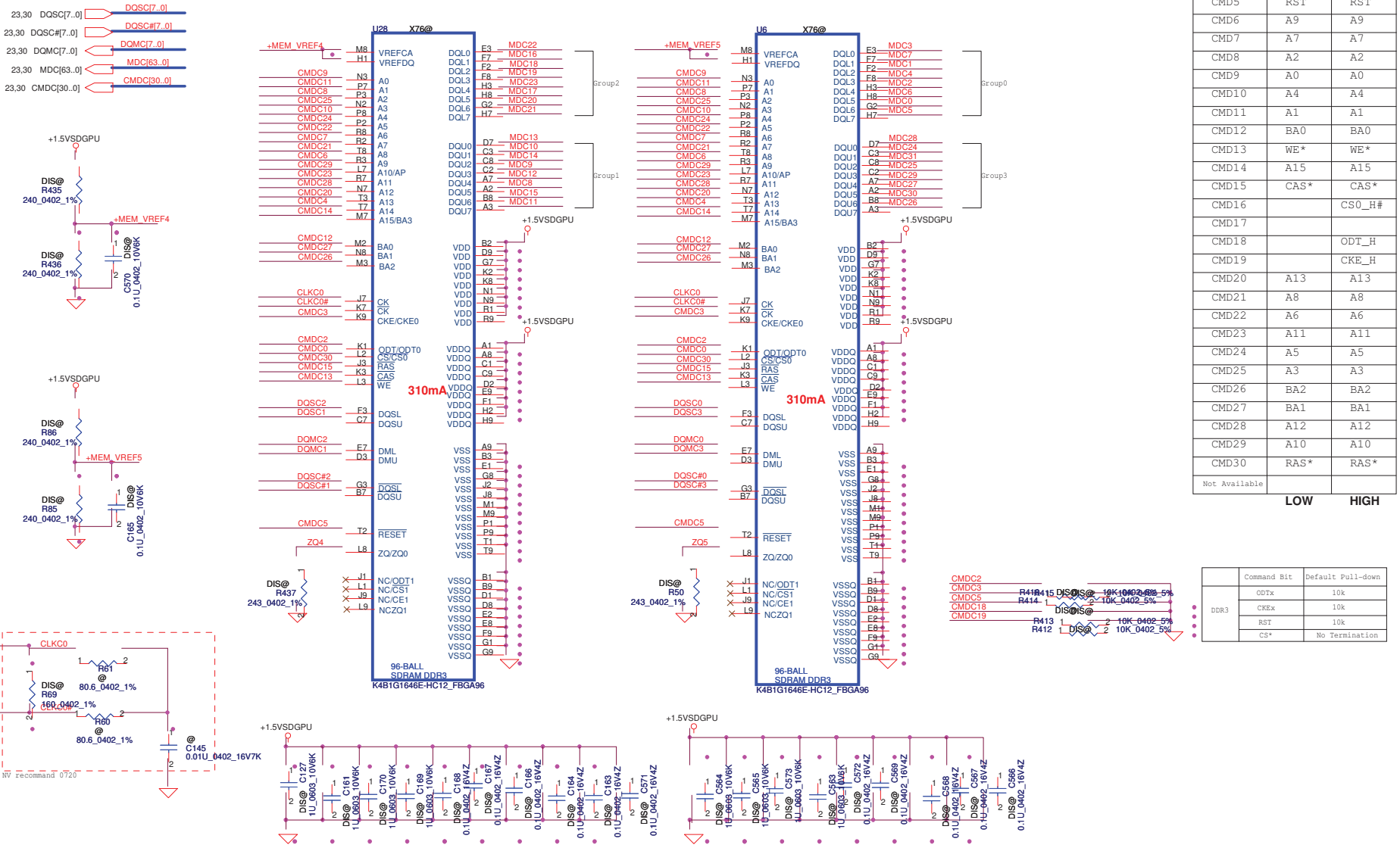
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: N12P DDR3 8/9

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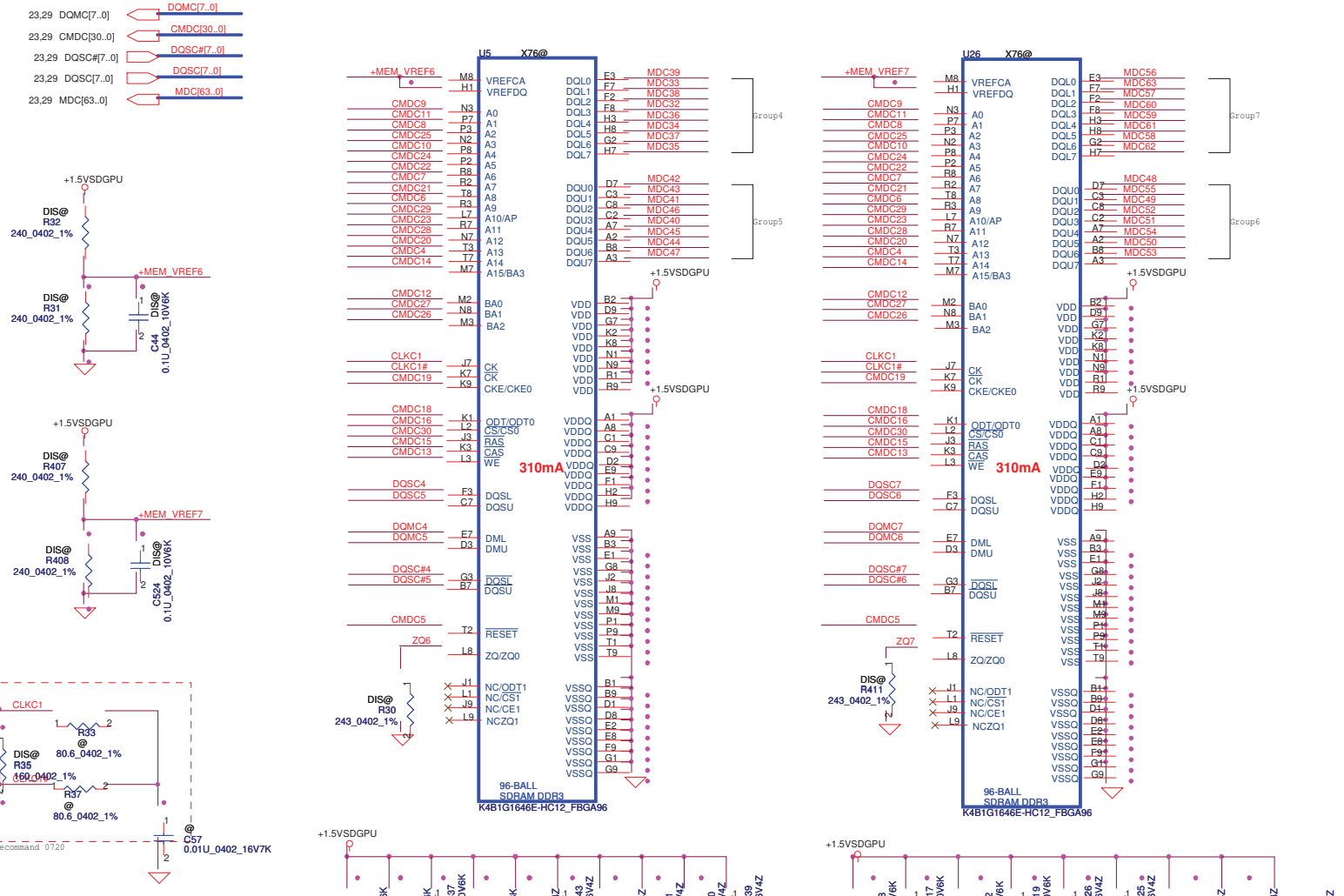
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.			
Title	N12P DDR3 9/9		
Size	Document Number		Rev
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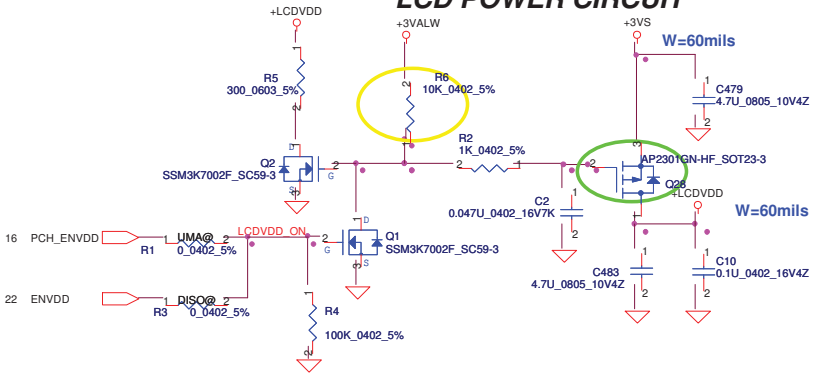
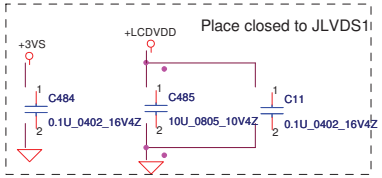
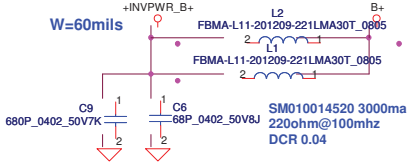
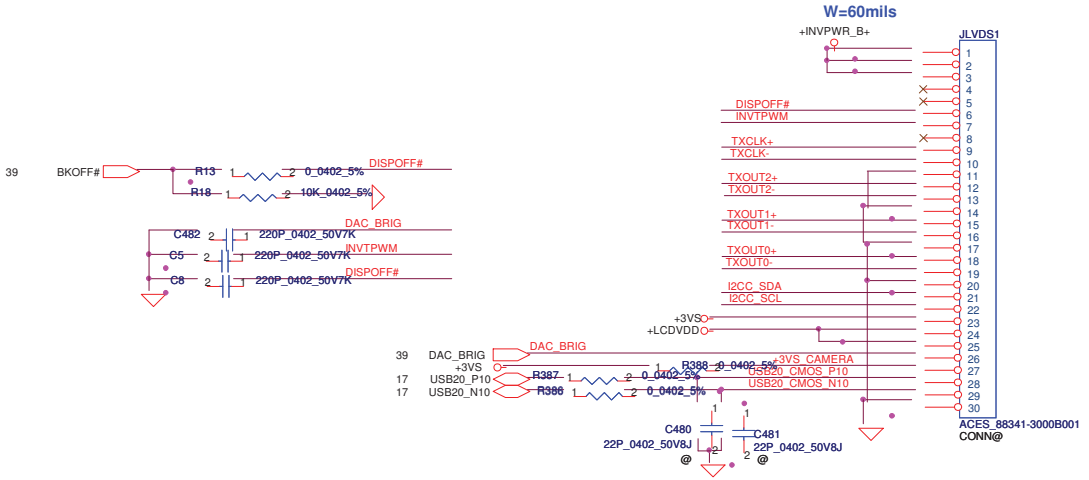
LCD POWER CIRCUIT



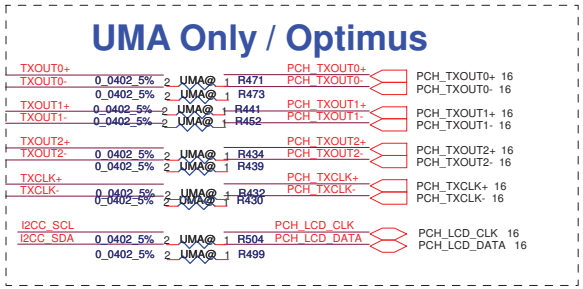




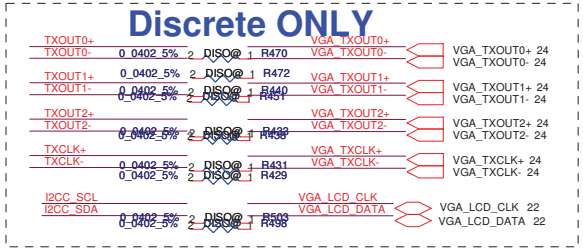
LCD/LED PANEL Conn.

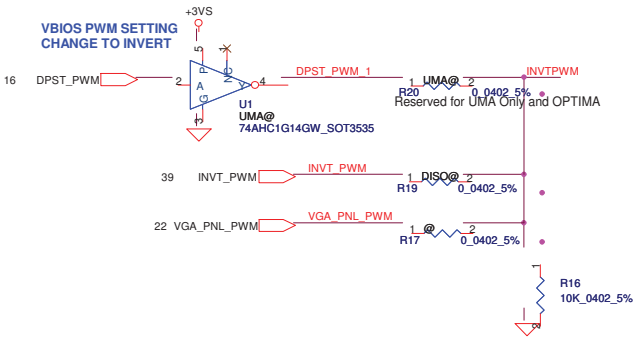


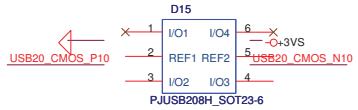
UMA Only / Optimus



Discrete ONLY







Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: LVDS Connector

Size	Document Number	Rev
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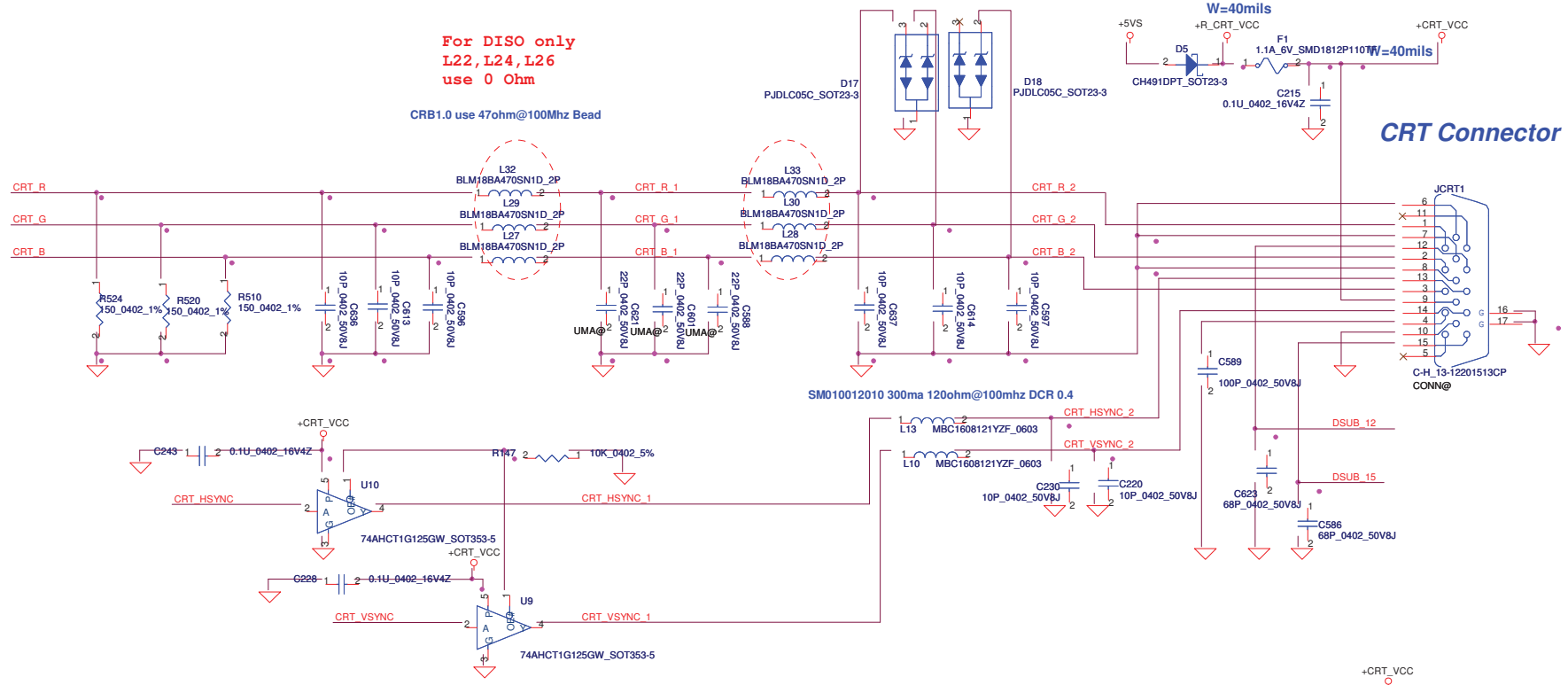

UMA Only / OPTIMUS

16	PCH_CRT_R	PCH_CRT_R	R420 2 UMA@ 1 0_0402_5%	CRT_R
16	PCH_CRT_G	PCH_CRT_G	R424 2 UMA@ 1 0_0402_5%	CRT_G
16	PCH_CRT_B	PCH_CRT_B	R422 2 UMA@ 1 0_0402_5%	CRT_B
16	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R428 2 UMA@ 1 33_0402_5%	CRT_HSYNC
16	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R426 2 UMA@ 1 33_0402_5%	CRT_VSYNC
16	PCH_CRT_CLK	PCH_CRT_CLK	R506 2 UMA@ 1 0_0402_5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH_CRT_DATA	R501 2 UMA@ 1 0_0402_5%	CRT_DDC_DATA

Discrete only

22	VGA_CRT_R	VGA_CRT_R	R419 2 DISO@ 1 0_0402_5%	CRT_R
22	VGA_CRT_G	VGA_CRT_G	R423 2 DISO@ 1 0_0402_5%	CRT_G
22	VGA_CRT_B	VGA_CRT_B	R421 2 DISO@ 1 0_0402_5%	CRT_B
22	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R427 2 DISO@ 1 0_0402_5%	CRT_HSYNC
22	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R425 2 DISO@ 1 0_0402_5%	CRT_VSYNC
22	VGA_DDC_CLK	VGA_DDC_CLK	R505 2 DISO@ 1 0_0402_5%	CRT_DDC_CLK
22	VGA_DDC_DATA	VGA_DDC_DATA	R500 2 DISO@ 1 0_0402_5%	CRT_DDC_DATA

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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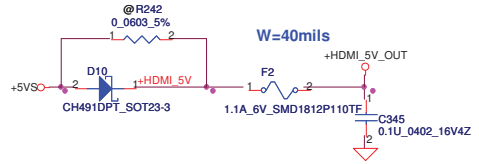
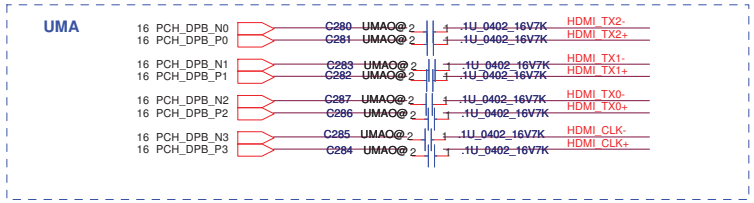
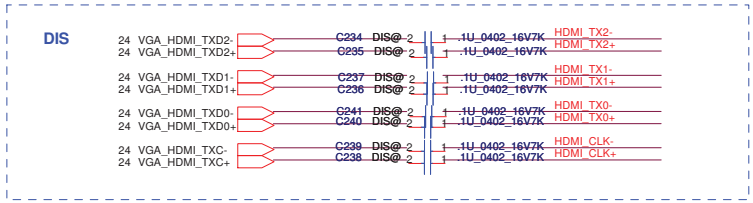
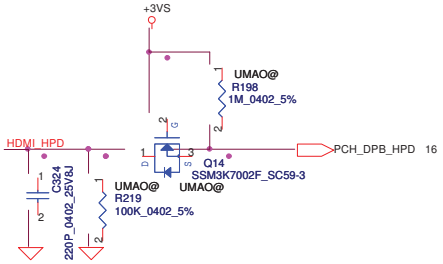
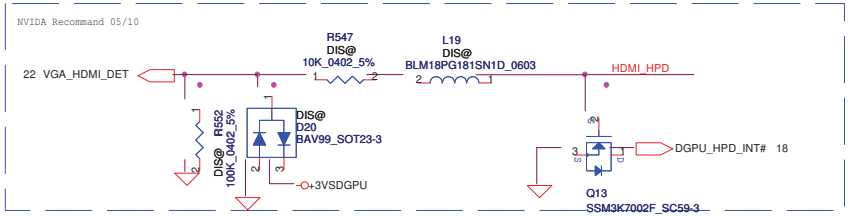


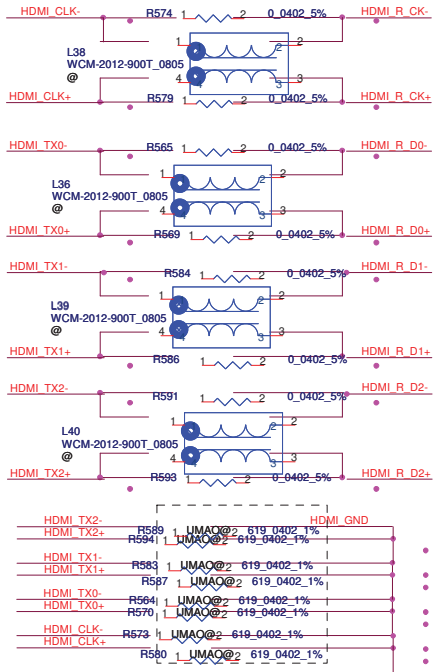




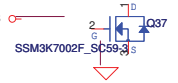




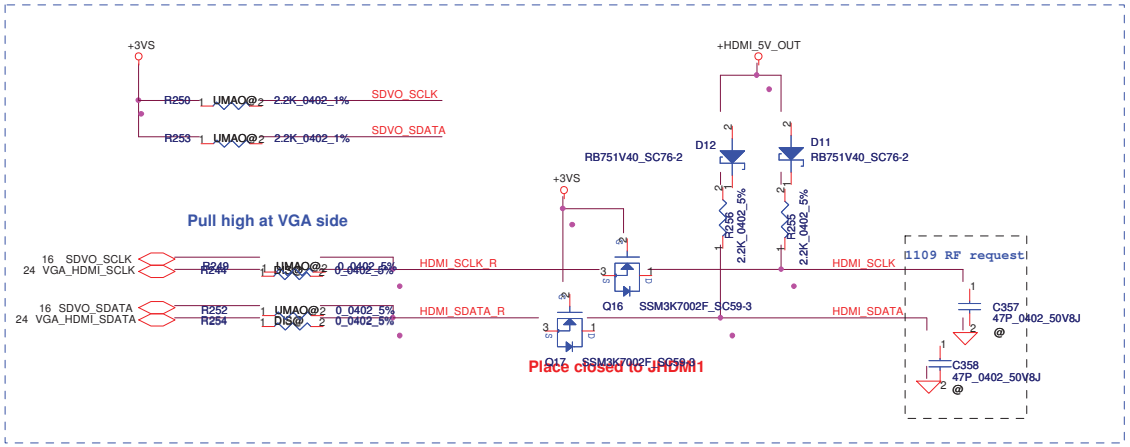
SM070001310 400ma 90ohm@100mhz DCR 0.3



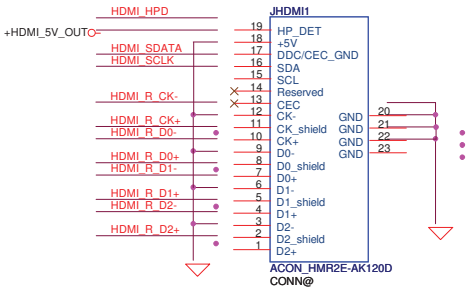
INTEL use 619 Ohm for terminationn



NV use 499 Ohm for terminationn



HDMI connector



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

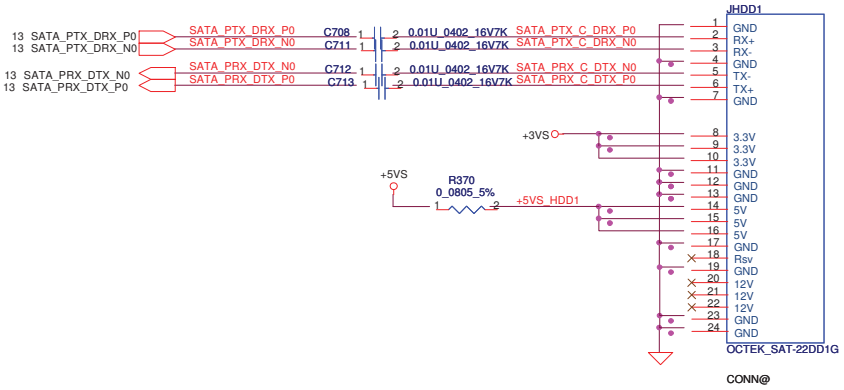
Compal Electronics, Inc.

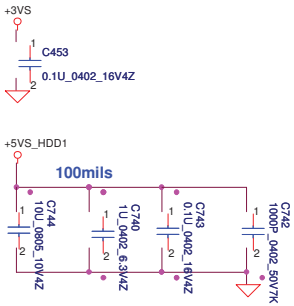
Title: HDMI Conn

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1
Date: Friday, August 27, 2010	Sheet 33 of 59	

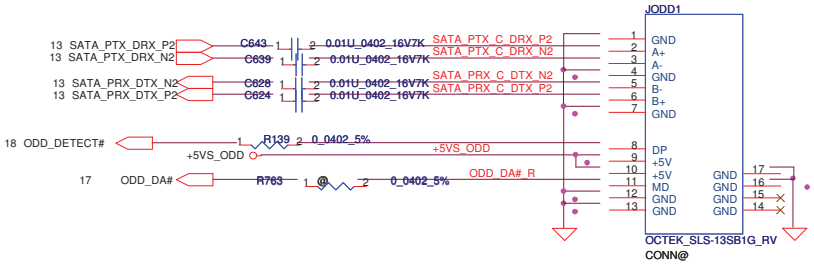
SATA HDD1 Conn.

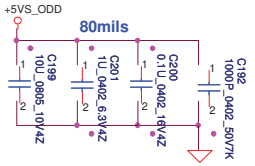
CL 4.0 mm

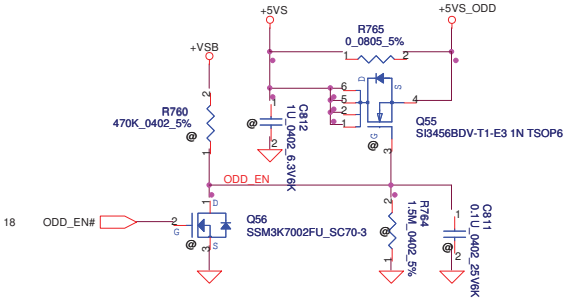




SATA ODD Conn.







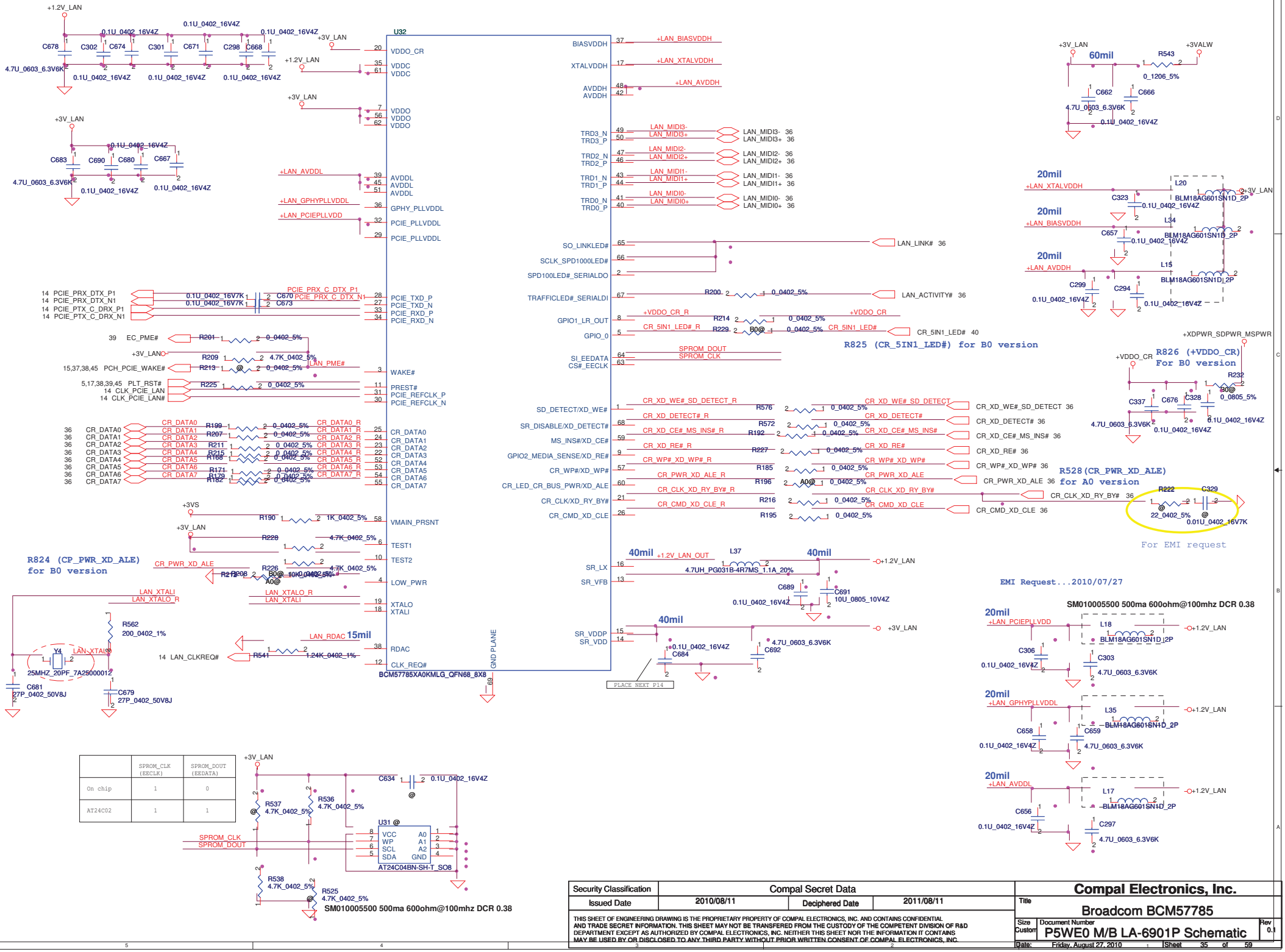
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 | Sheet 34 of 59



	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

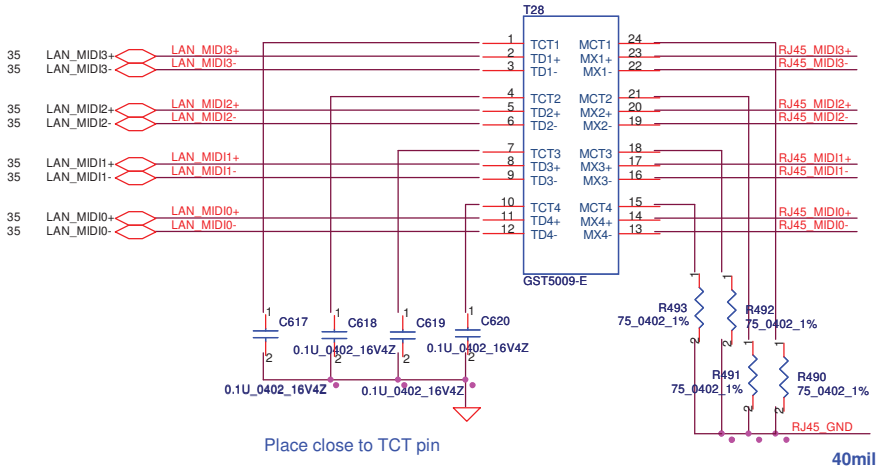
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: Broadcom BCM57785

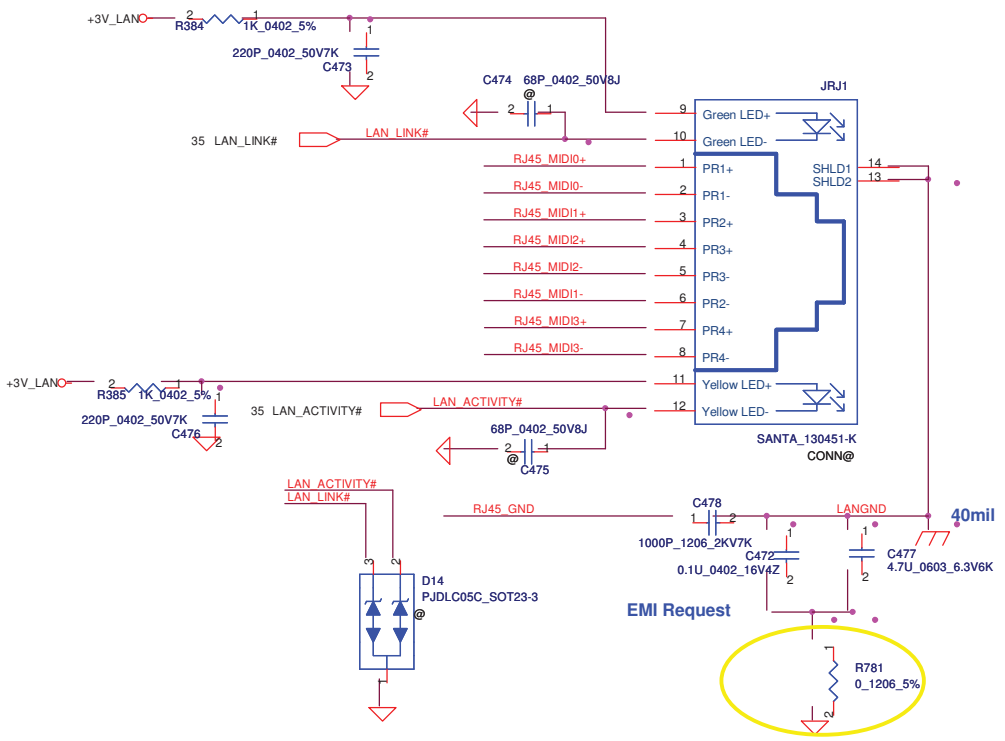
Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 | Sheet 35 of 59

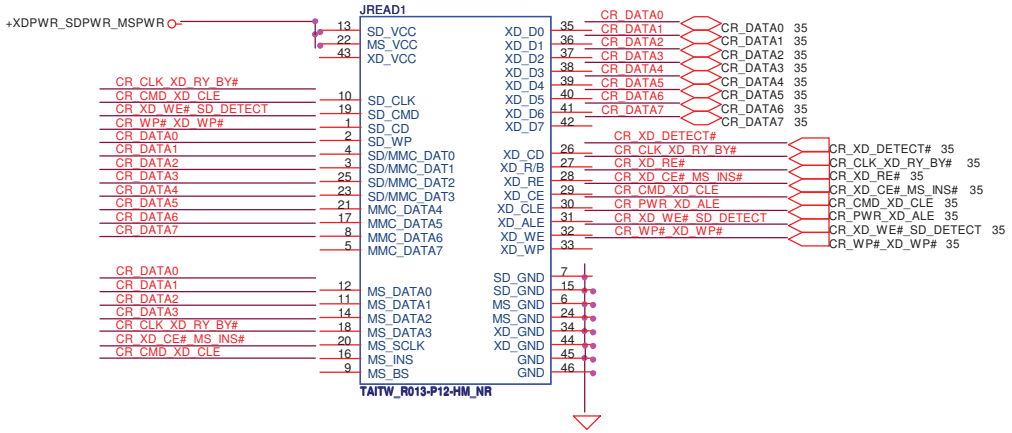


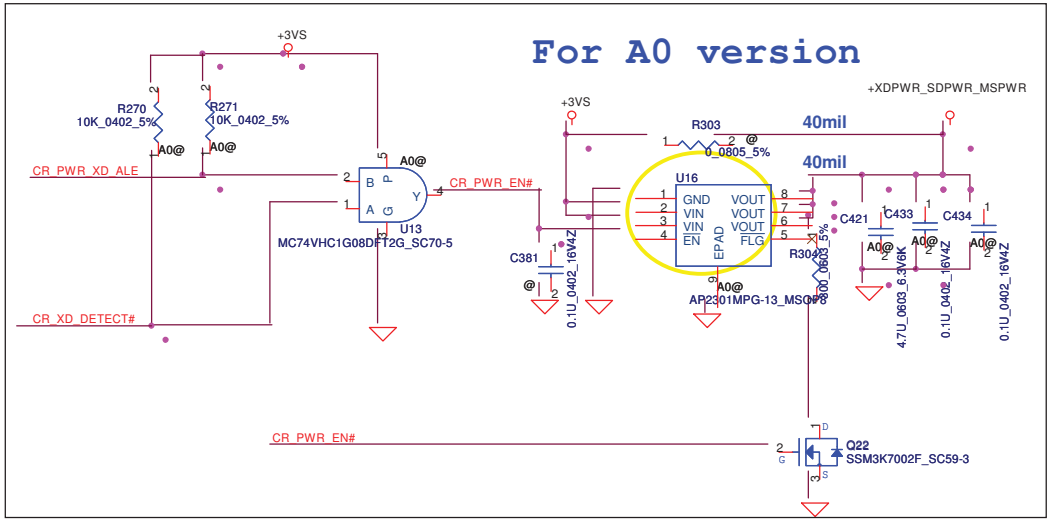
BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

LAN Connector



Card Reader Connector





Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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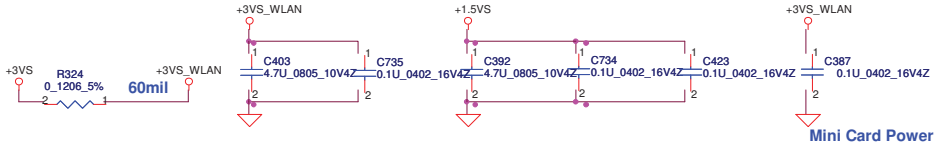
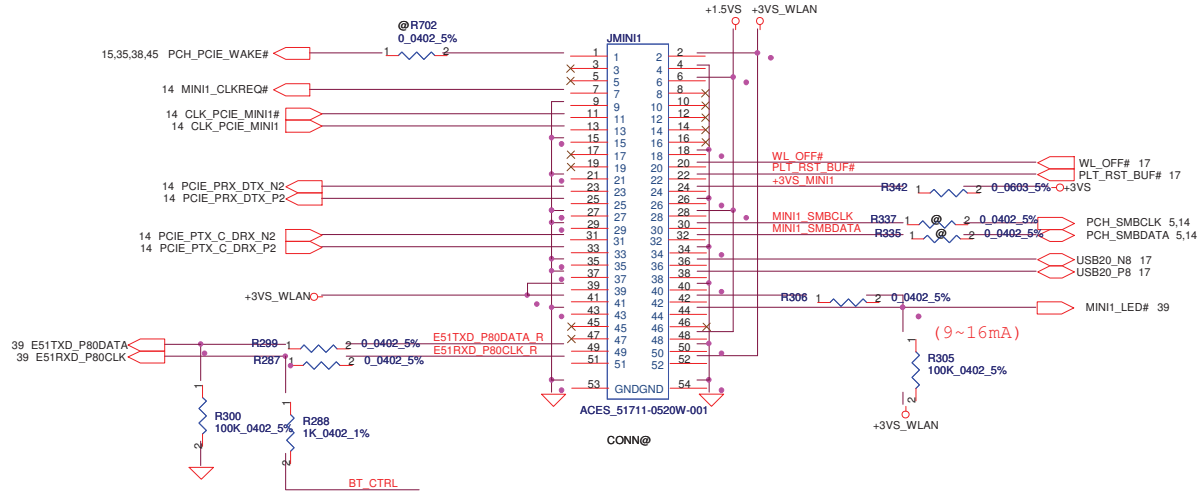
For Wireless LAN

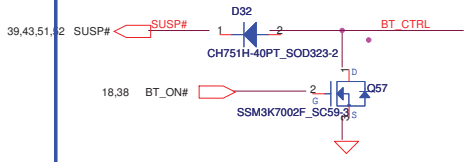


Mini Card Power Rating

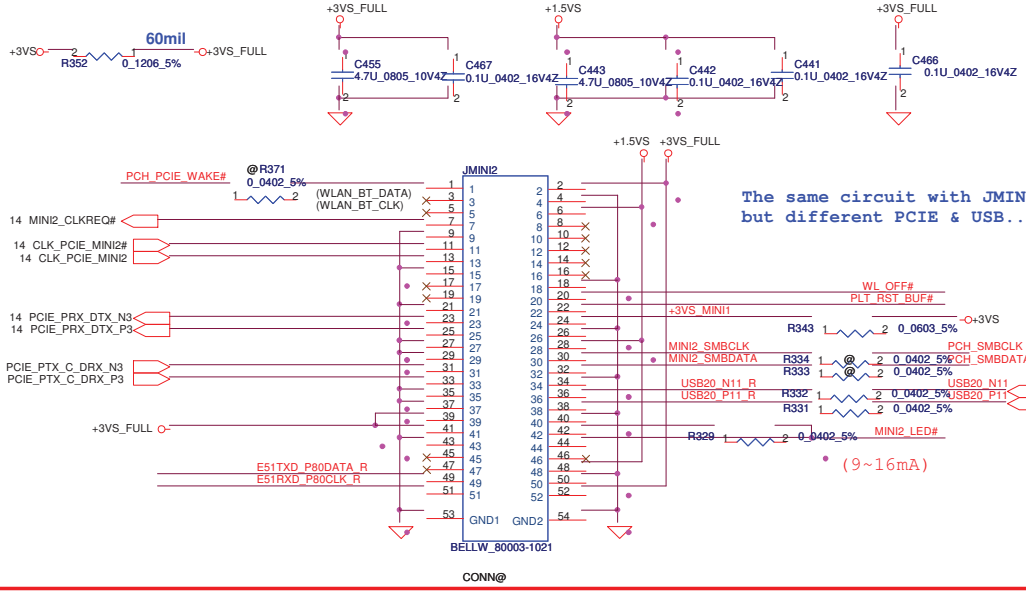


WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

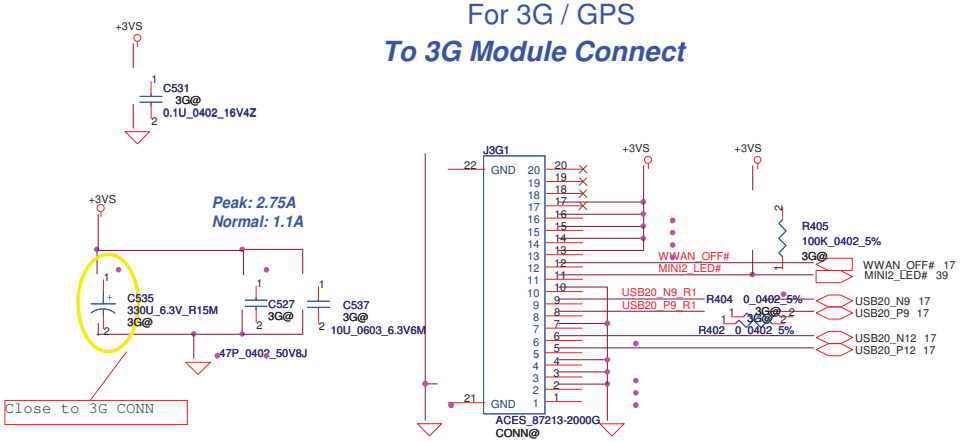


Reserve



For 3G / GPS

To 3G Module Connect



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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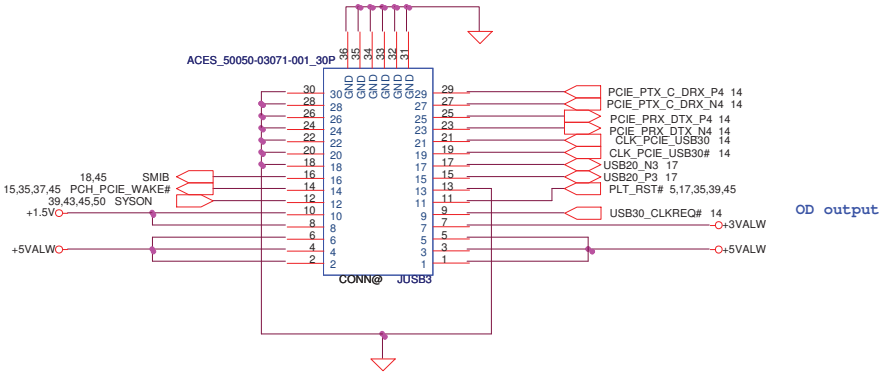
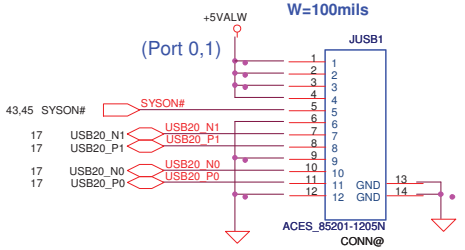
USB3.0 Conn.

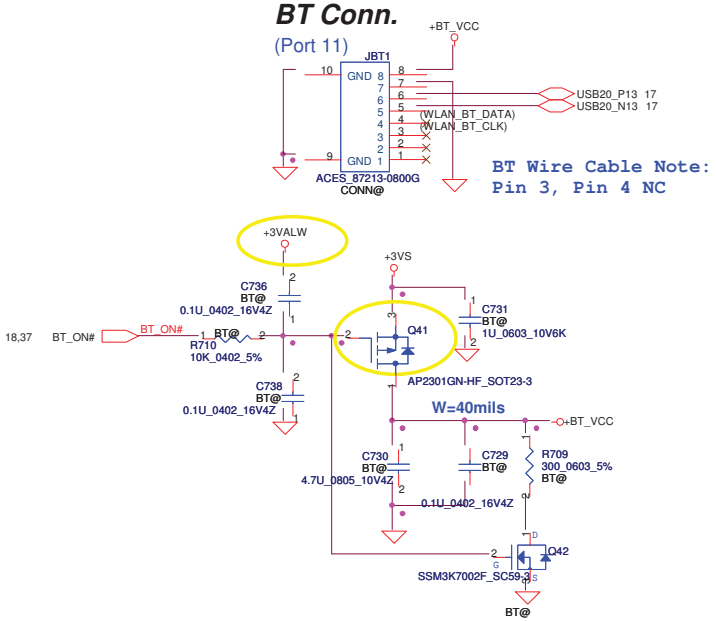


OD output

USB/B Conn.



BT Conn.



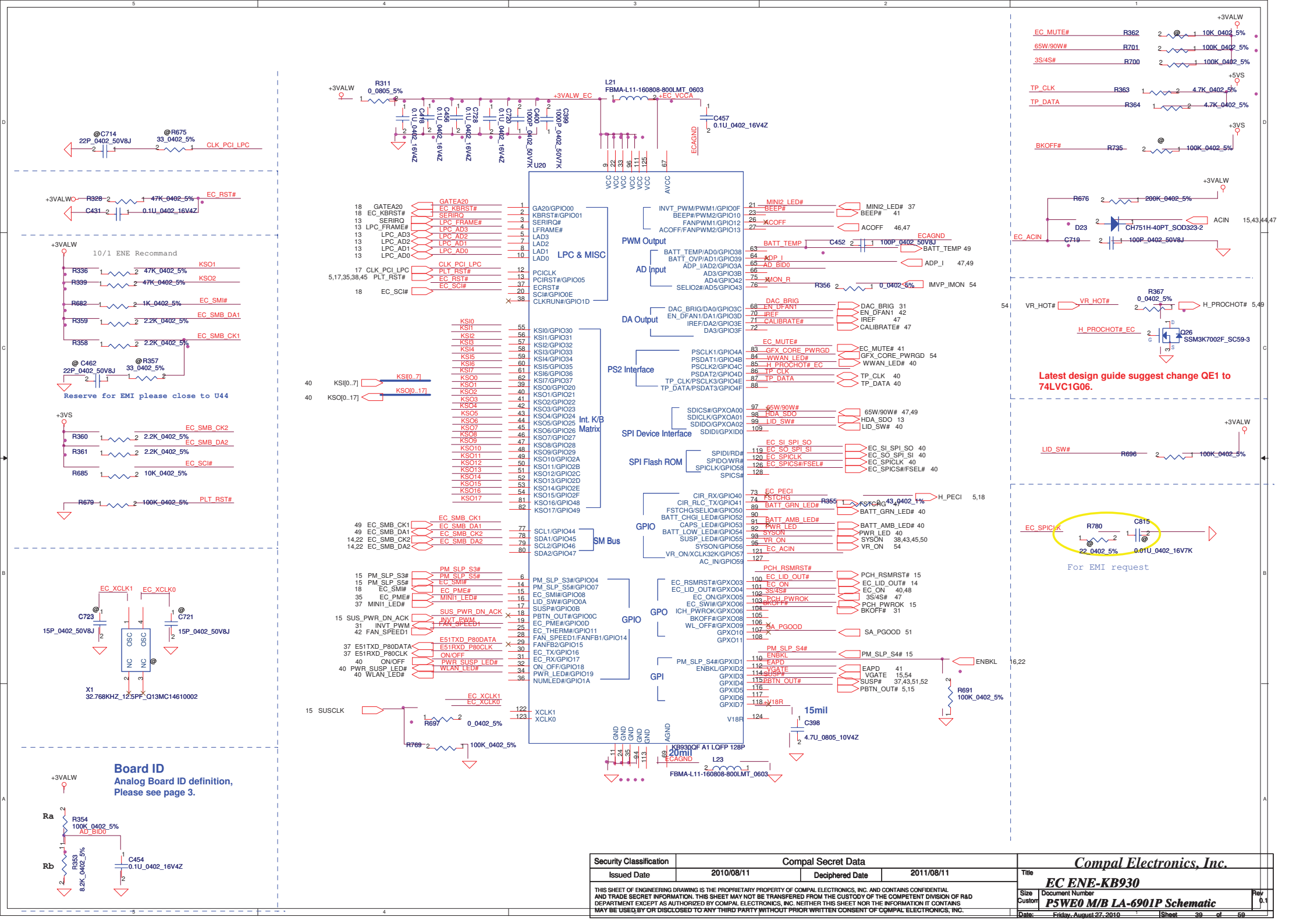
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: USB / BT / USBB

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

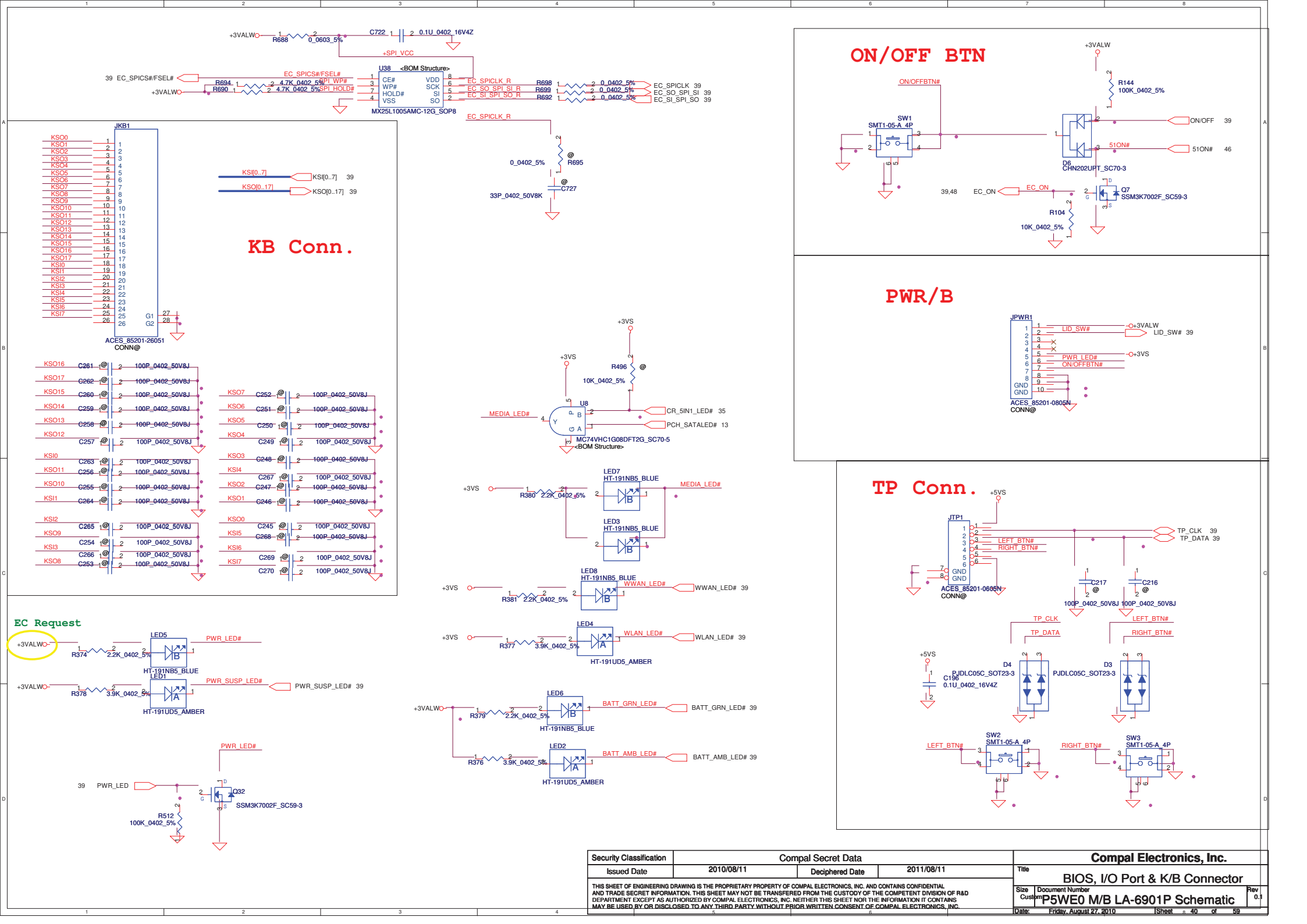
Date: Friday, August 27, 2010 | Sheet 38 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title	EC ENE-KB930	
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic	Rev: 0.1
Date: Friday, August 27, 2010	Sheet 39 of 59	



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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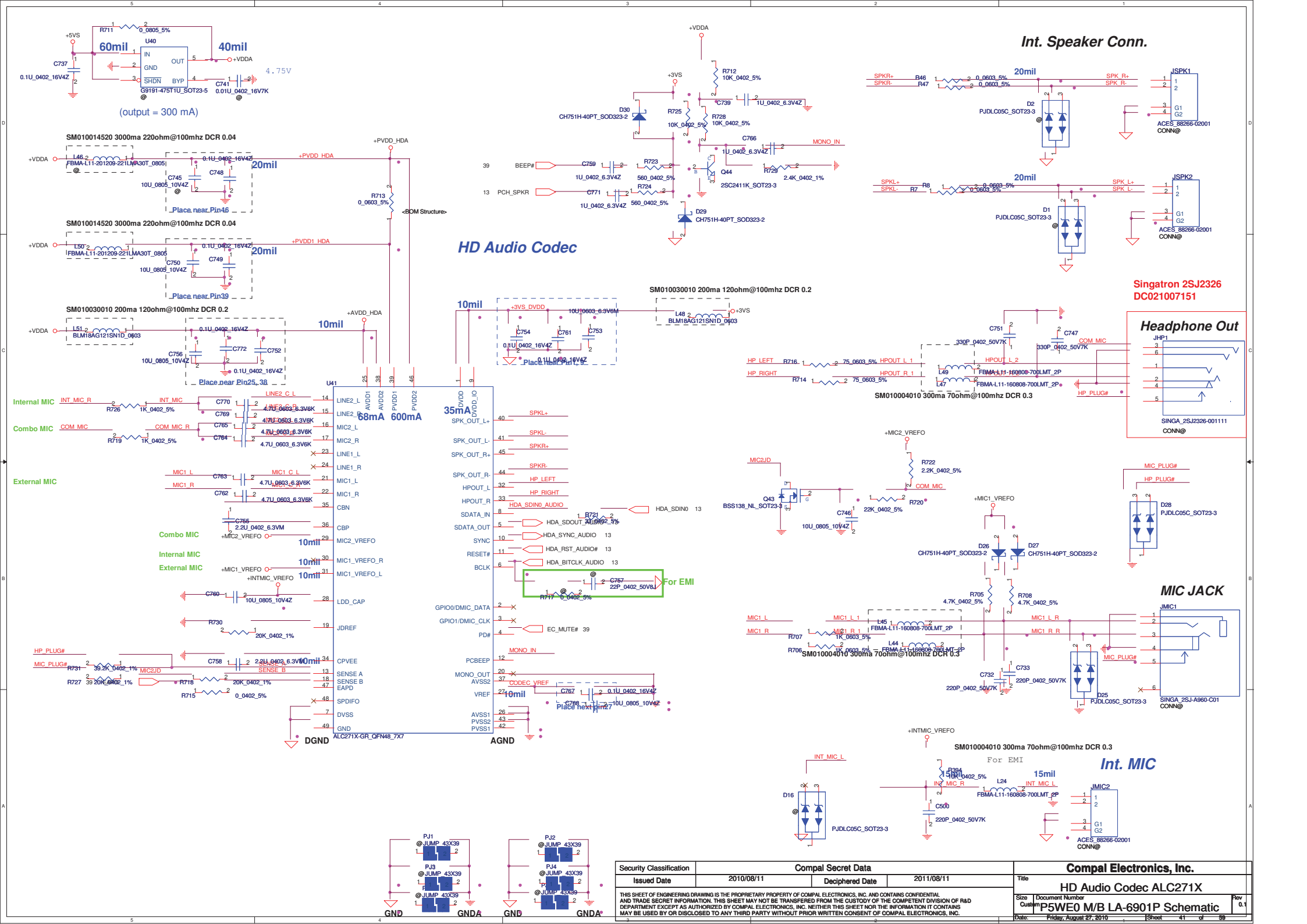

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: HD Audio Codec ALC271X

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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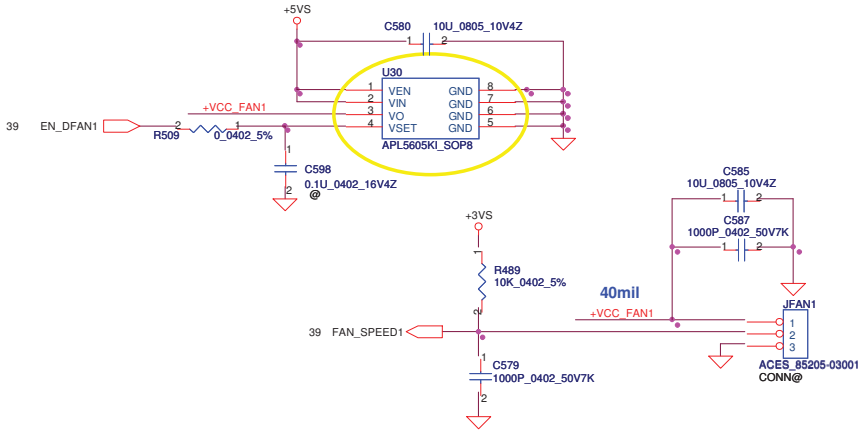
FAN Stand-Off

JUSB3 Stand-Off

H1 H_3P4 @
H2 H_3P4 @
H3 H_3P4 @
H4 H_3P4 @
H5 H_3P4 @
H6 H_3P4 @
H7 H_3P4 @
H8 H_3P0 @
H9 H_3P0 @
H10 H_3P0 @
H11 H_3P0 @
H12 H_3P0 @
H13 H_3P0 @
H14 H_3P0 @
H15 H_3P0 @
H16 H_3P0 @
H17 H_3P0 @
H18 H_3P0 @
H19 H_4P0 @
H20 H_4P0 @
H21 H_4P2 @
H22 H_4P2 @
H23 H_4P2 @
H24 H_4P2 @
H25 H_7P0N @
H26 H_3P0N @
H27 H_3P5X3P0N @

FAN1 Conn



FD1 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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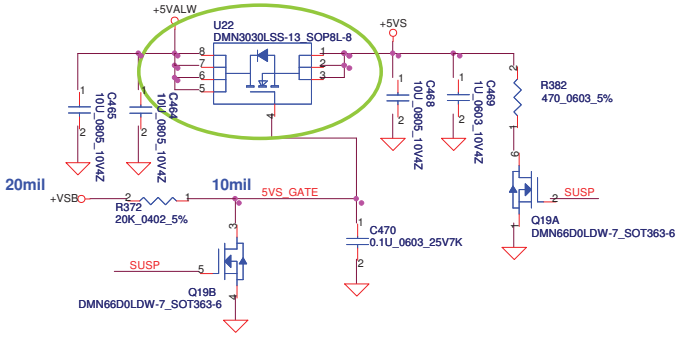
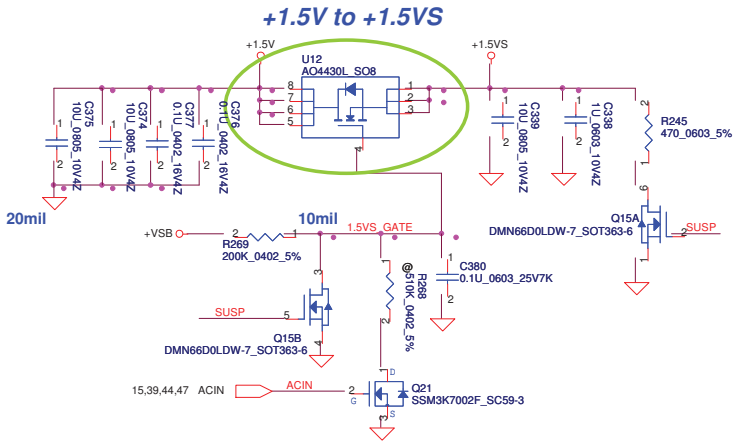
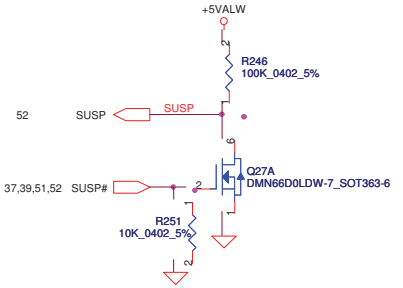
+5VALW TO +5VS

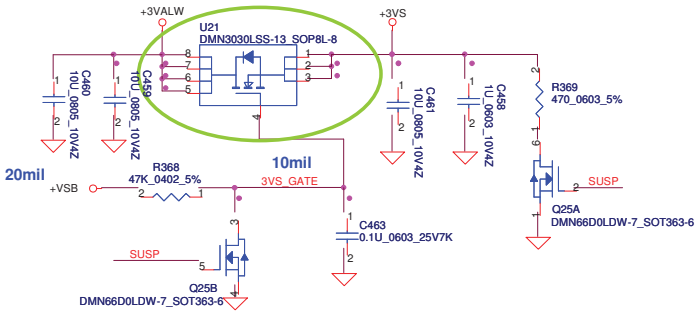


+1.5V to +1.5VS

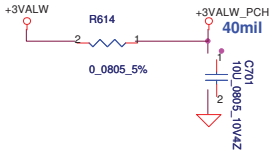


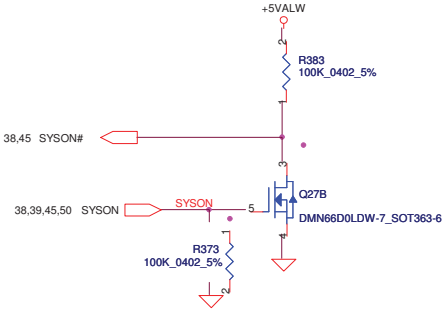


+3VALW TO +3VS

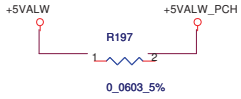


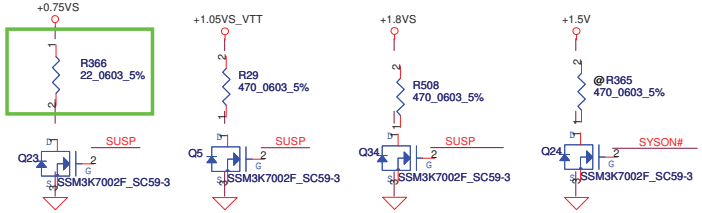
+3VALW TO +3VALW_PCH(PCH AUX Power)





+5VALW TO +5VALW_PCH(PCH AUX Power)





Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

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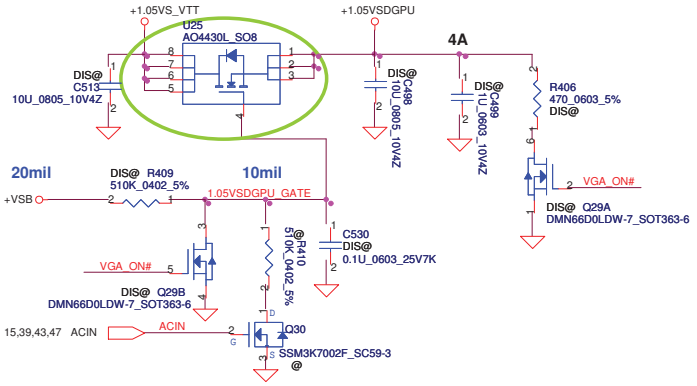
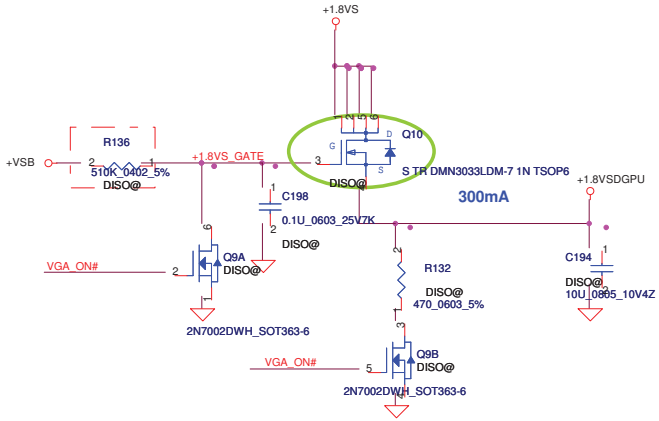
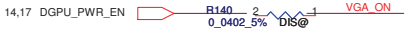
+1.05VS_VTT to +1.05VSDGPU for GPU

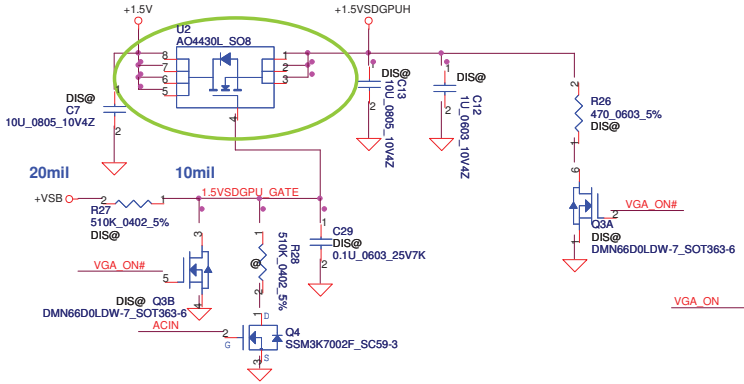


+1.8VS to +1.8VSDGPU for GPU

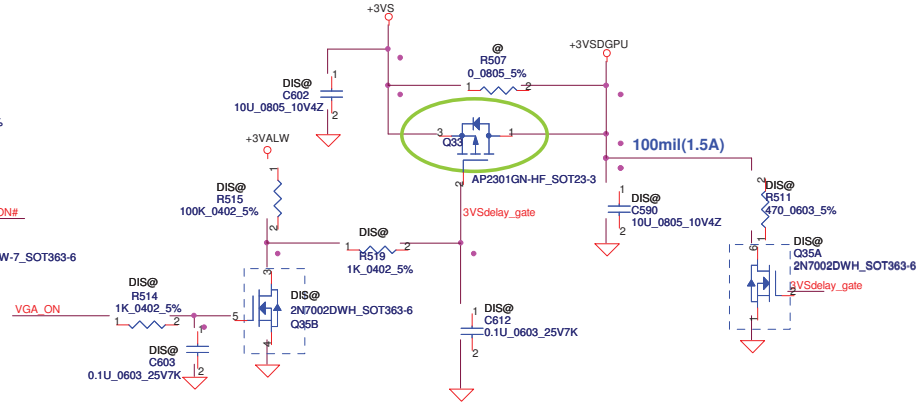


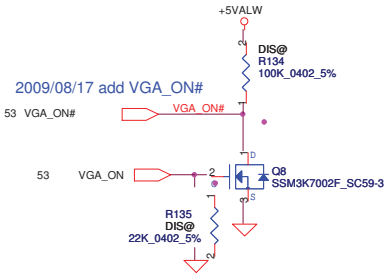


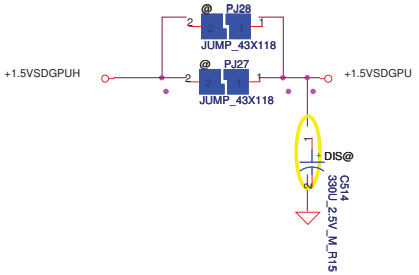
+1.5V to +1.5VSDGPUH for GPU



+3VS to +3VSDGPU for GPU







Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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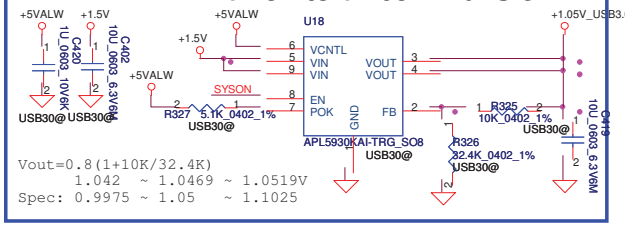
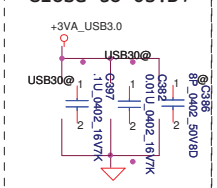
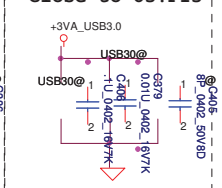
+1.5V to +1.05V Transfer

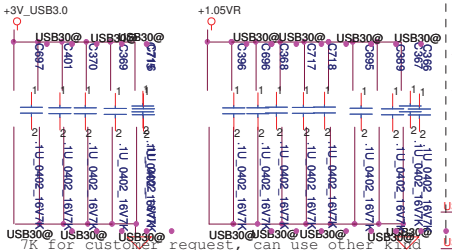


Close to U3.D7

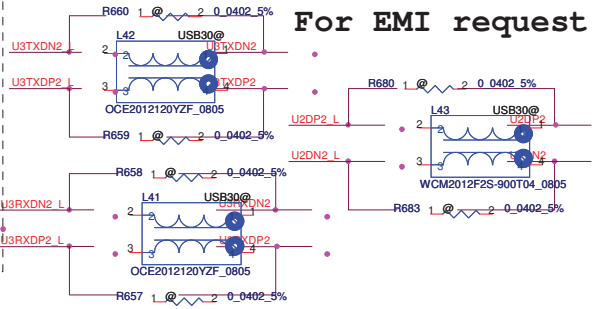


Close to U3.P13

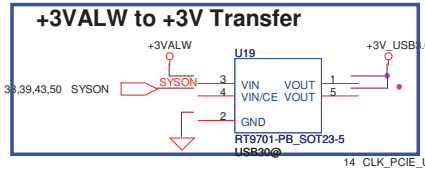


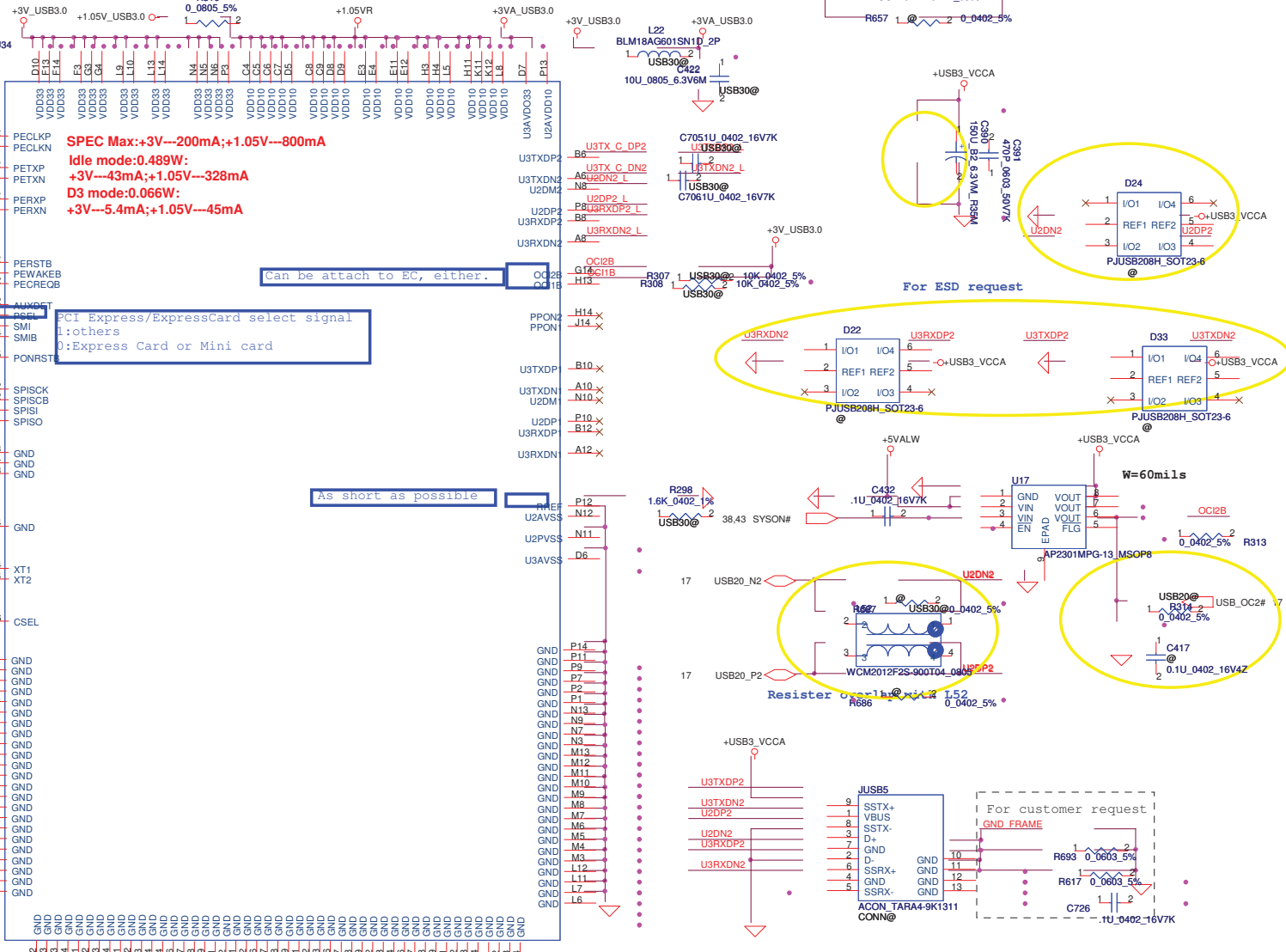


For EMI request



+3VALW to +3V Transfer





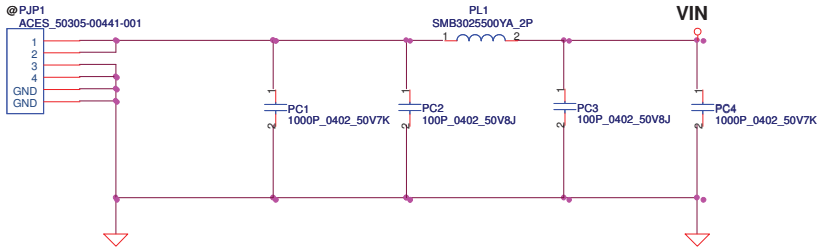
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

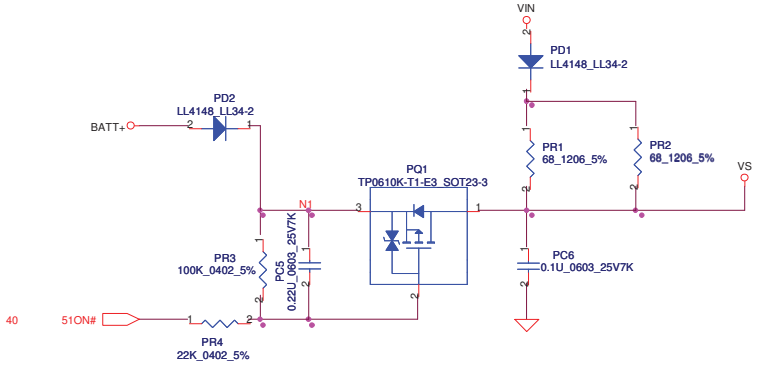
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

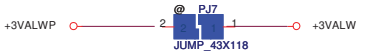
Title: **USB3.0 PD720200**

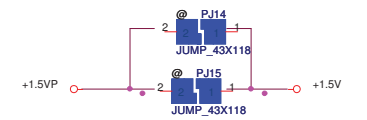
Size	Document Number	Rev
Custom		0.1

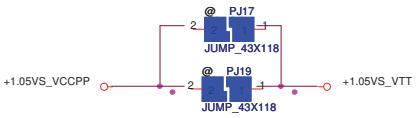
Date: Friday, August 27, 2010 Sheet 45 of 59

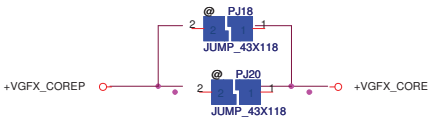


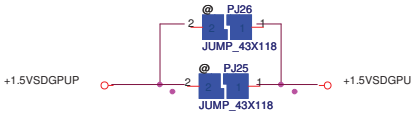


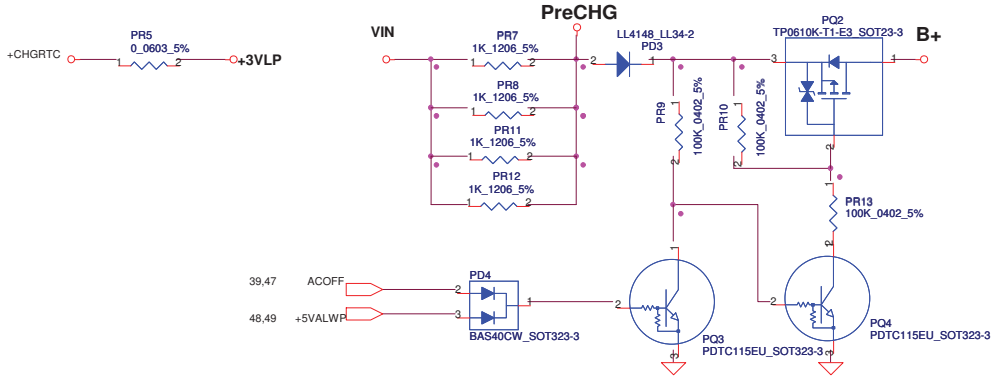












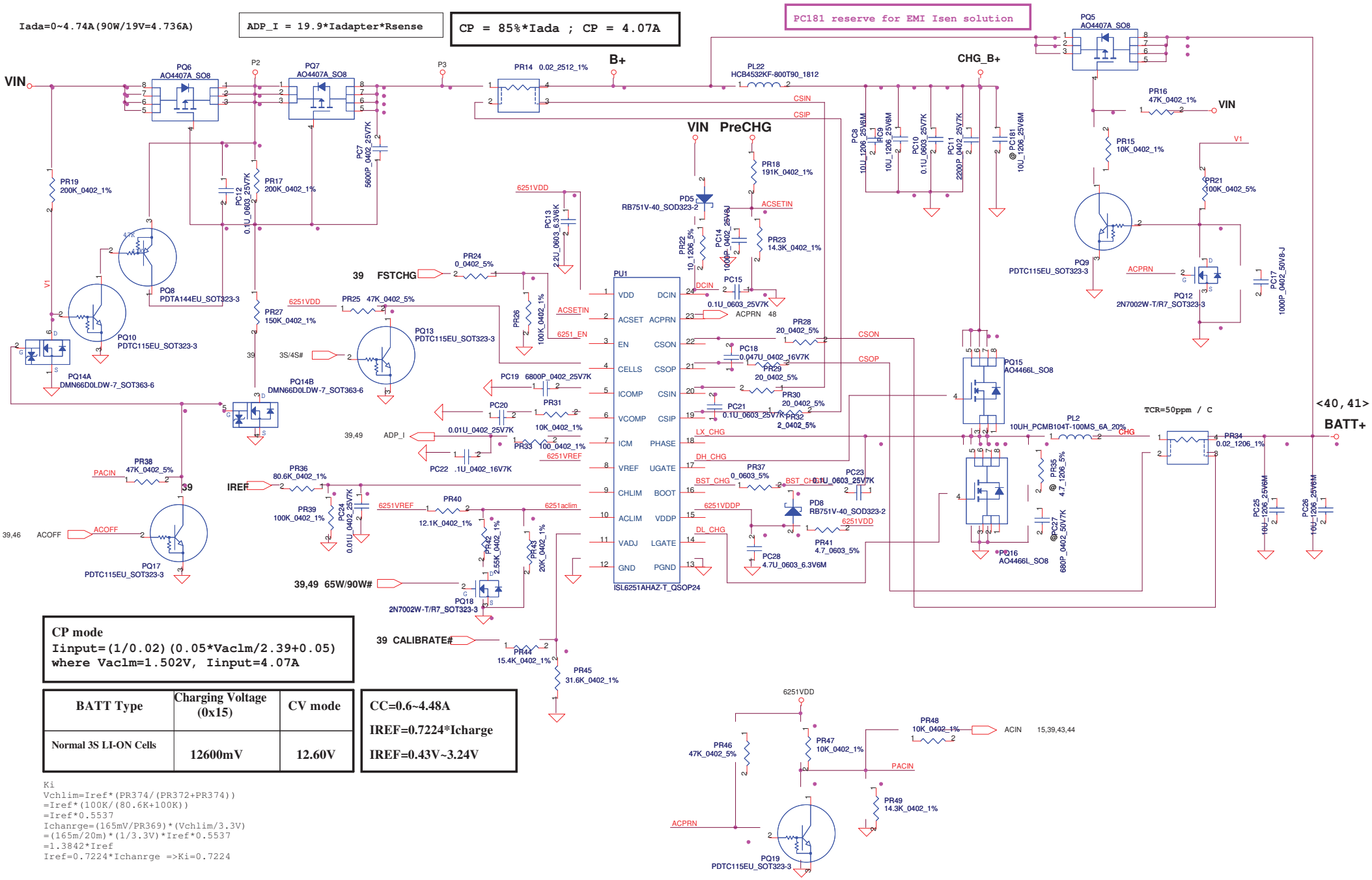
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 46 of 59



CP mode

$$I_{input} = (1/0.02)(0.05 * V_{aclm}/2.39 + 0.05)$$

where $V_{aclm} = 1.502V$, $I_{input} = 4.07A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki

Vchlim=Iref*(PR374/(PR372+PR374))

=Iref*(100K/(80.6K+100K))

=Iref*0.5537

Ichanrge=(165mV/PR369)*(Vchlim/3.3V)

=(165m/20m)*(1/3.3V)*Iref*0.5537

=1.3842*Iref

Iref=0.7224*Ichanrge =>Ki=0.7224

Kv

Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K

R=514K//31.6K//(15.4K+3k)=11.372K

r=514K//514K//31.6K=28.14K

Vcell=0.175*Vadj+3.99v

4.2V=0.175*Vadj+3.99V =>Vadj=1.2V

Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))

1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899

1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv

A=Vref*(R/(R+514K))=0.052

Kv=9.451

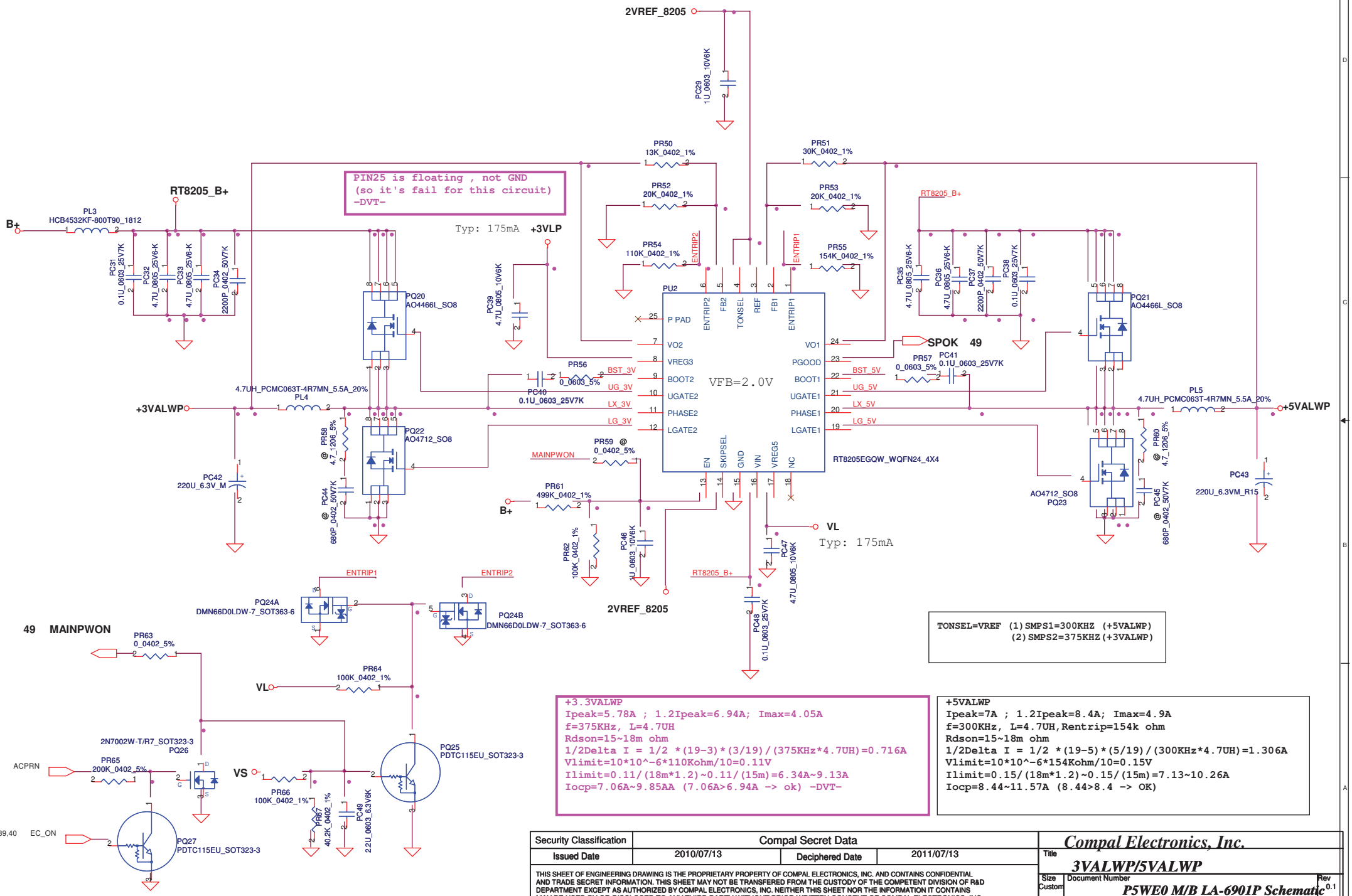
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 47 of 59



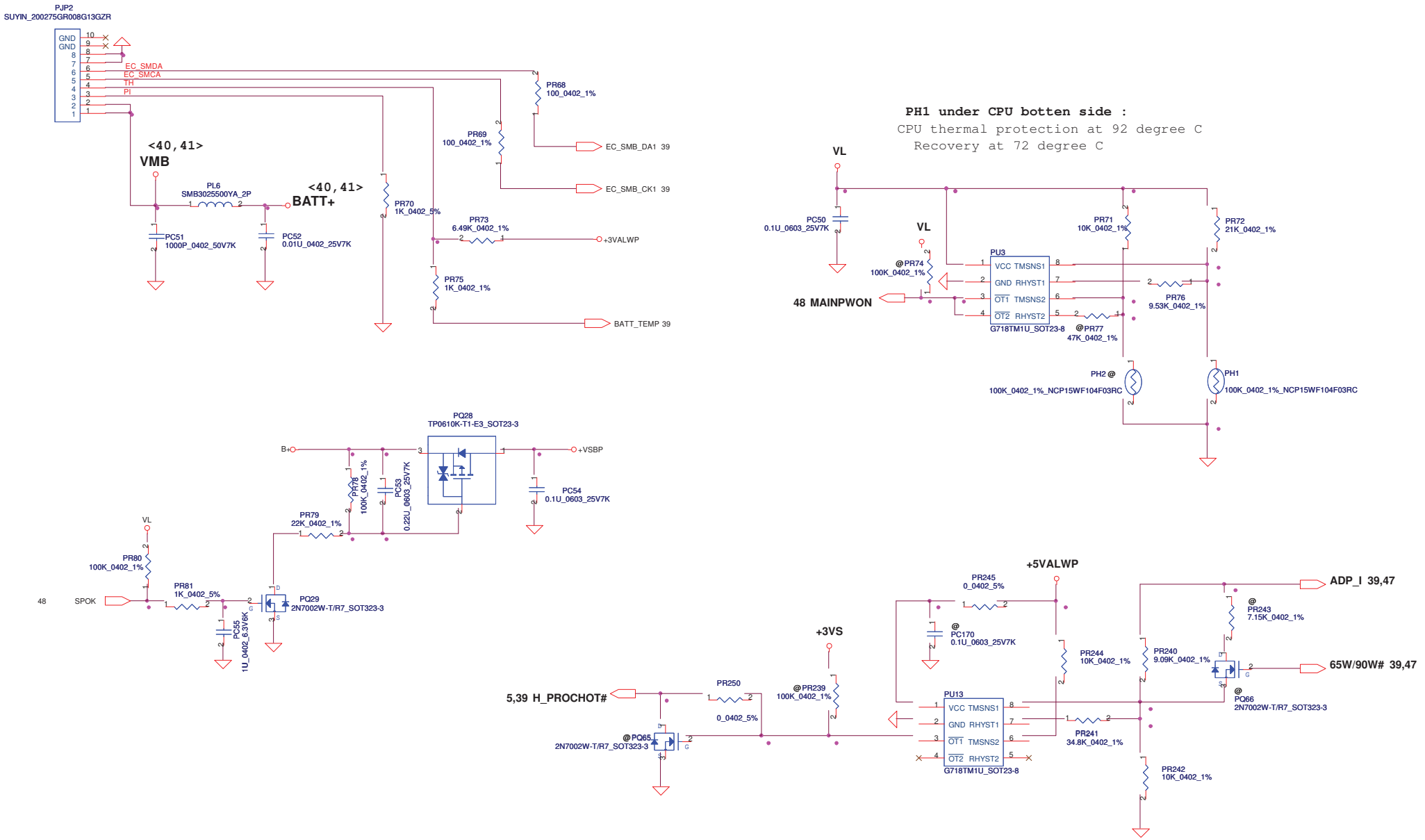
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 48 of 59



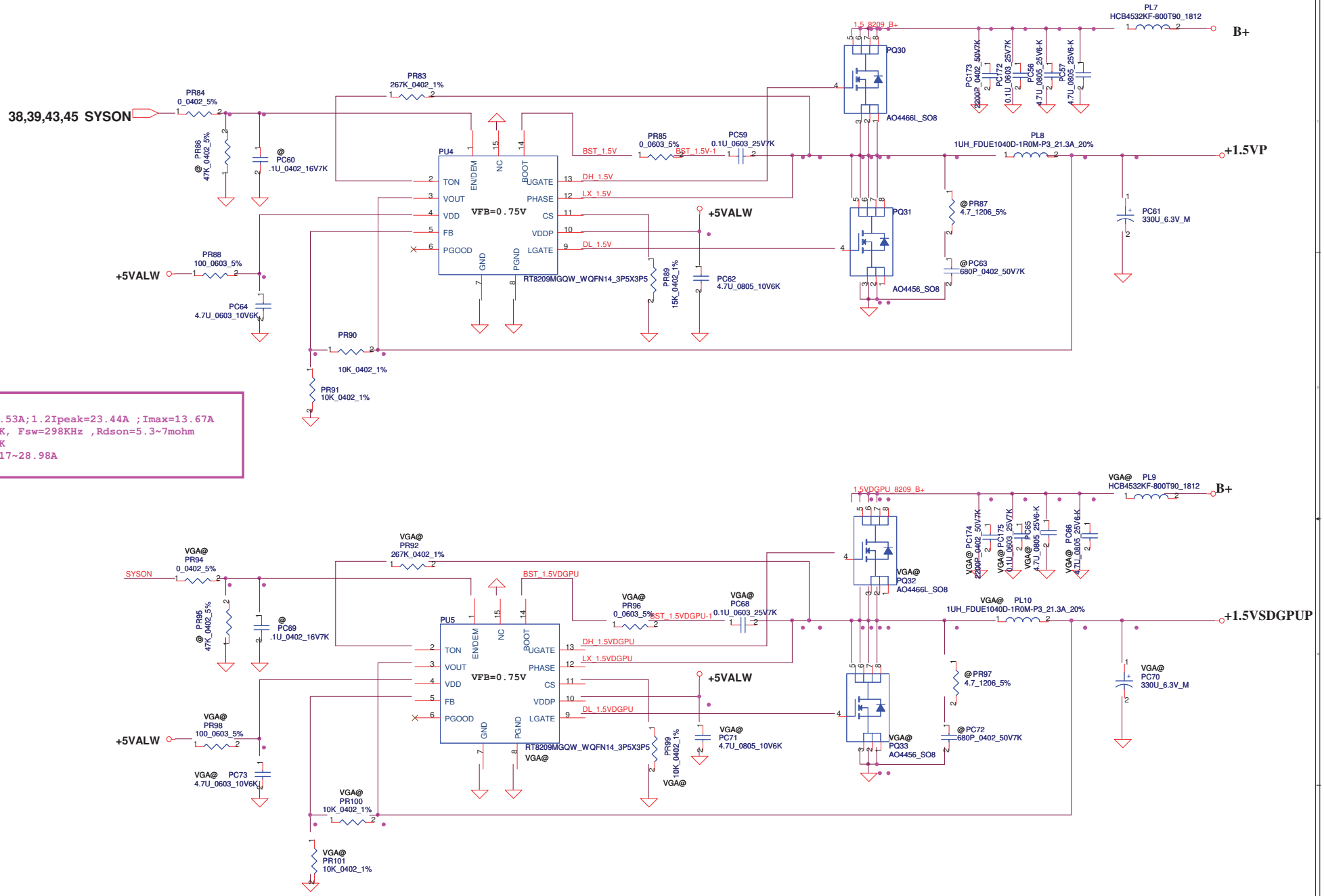
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 49 of 59



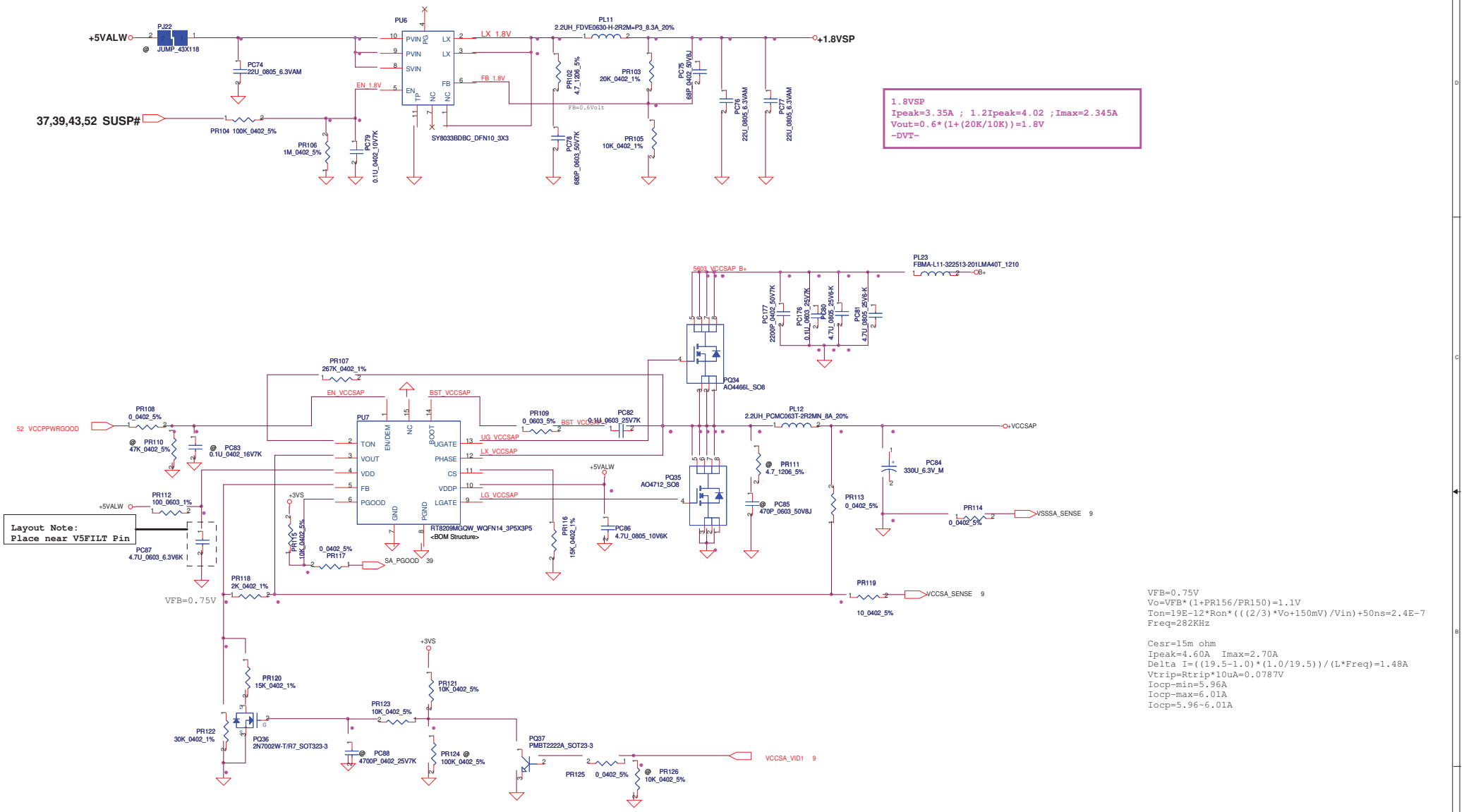
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.5VSDGPU

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 50 of 59



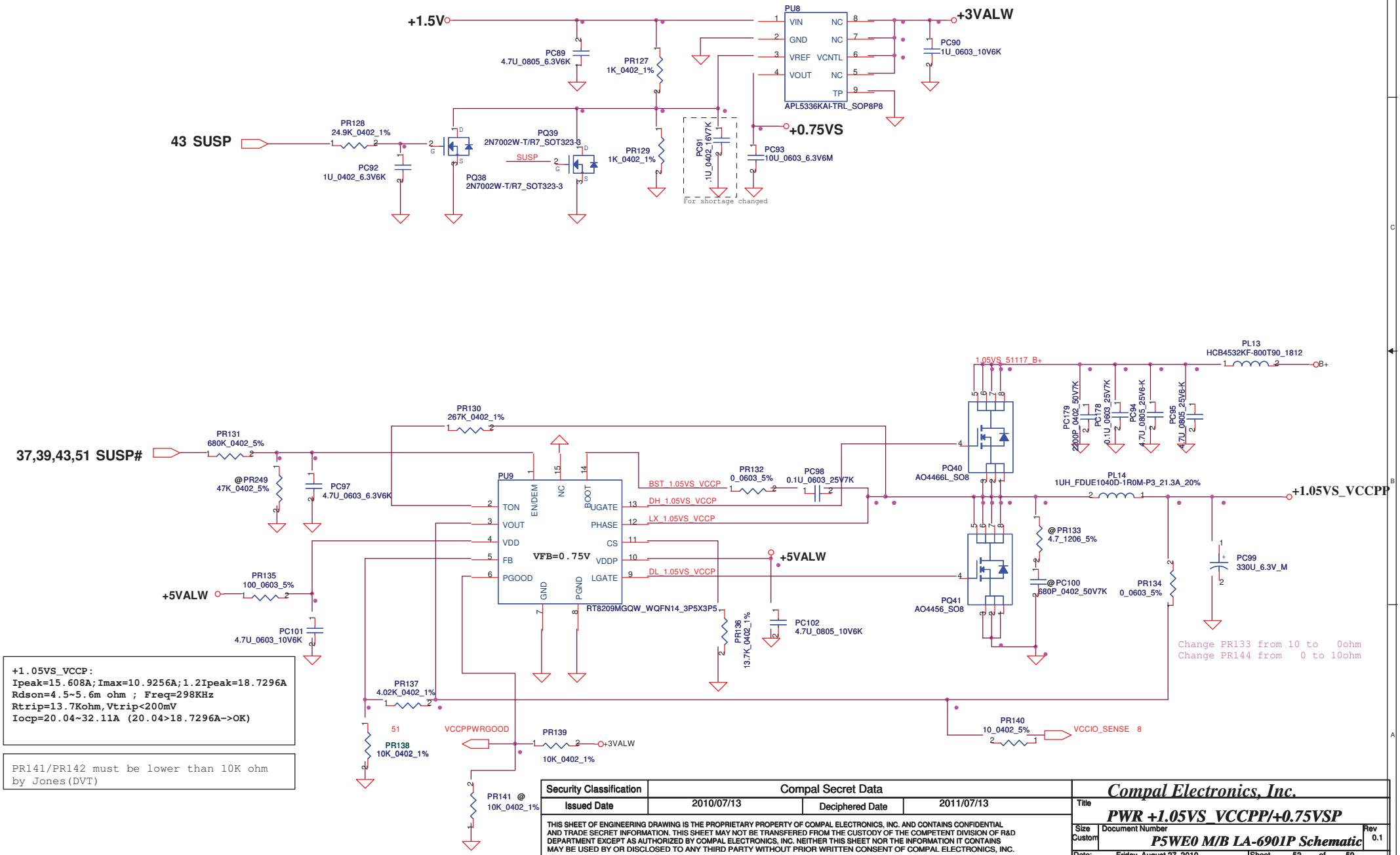
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size: C | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 51 of 58



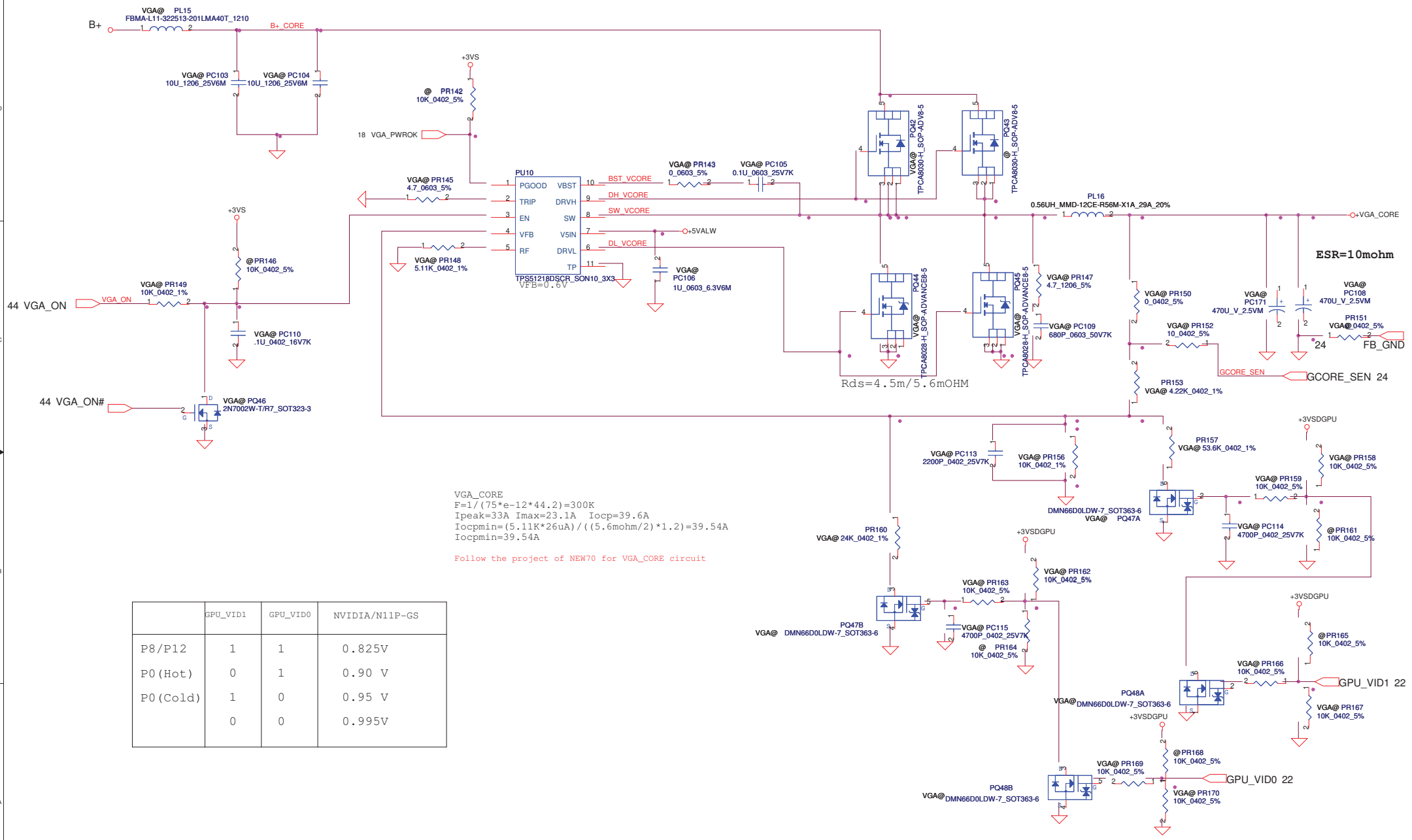
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 52 of 59



VGA_CORE
F=1/(75*e-12*44.2)=300K
Ipeak=33A Imax=23.1A Iocp=39.6A
Iocpmin=(5.11K*26uA)//((5.6mohm/2)*1.2)=39.54A
Iocpmin=39.54A

Follow the project of NEW70 for VGA_CORE circuit

	GPU_VID1	GPU_VID0	NVIDIA/N11P-GS
P8/P12	1	1	0.825V
P0(Hot)	0	1	0.90 V
P0(Cold)	1	0	0.95 V
	0	0	0.995V

Security Classification	Compal Secret Data		AP
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: +VGA_COREP

Size	Document Number	Rev
Custom	P5WE0	0.1

Date: Friday, August 27, 2010 Sheet 53 of 59

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

change from 680P to 470P
for shortage problem
2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR +CPU_CORE/+VGFX_CORE

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 54 of 59

Version change list (P.I.R. List)

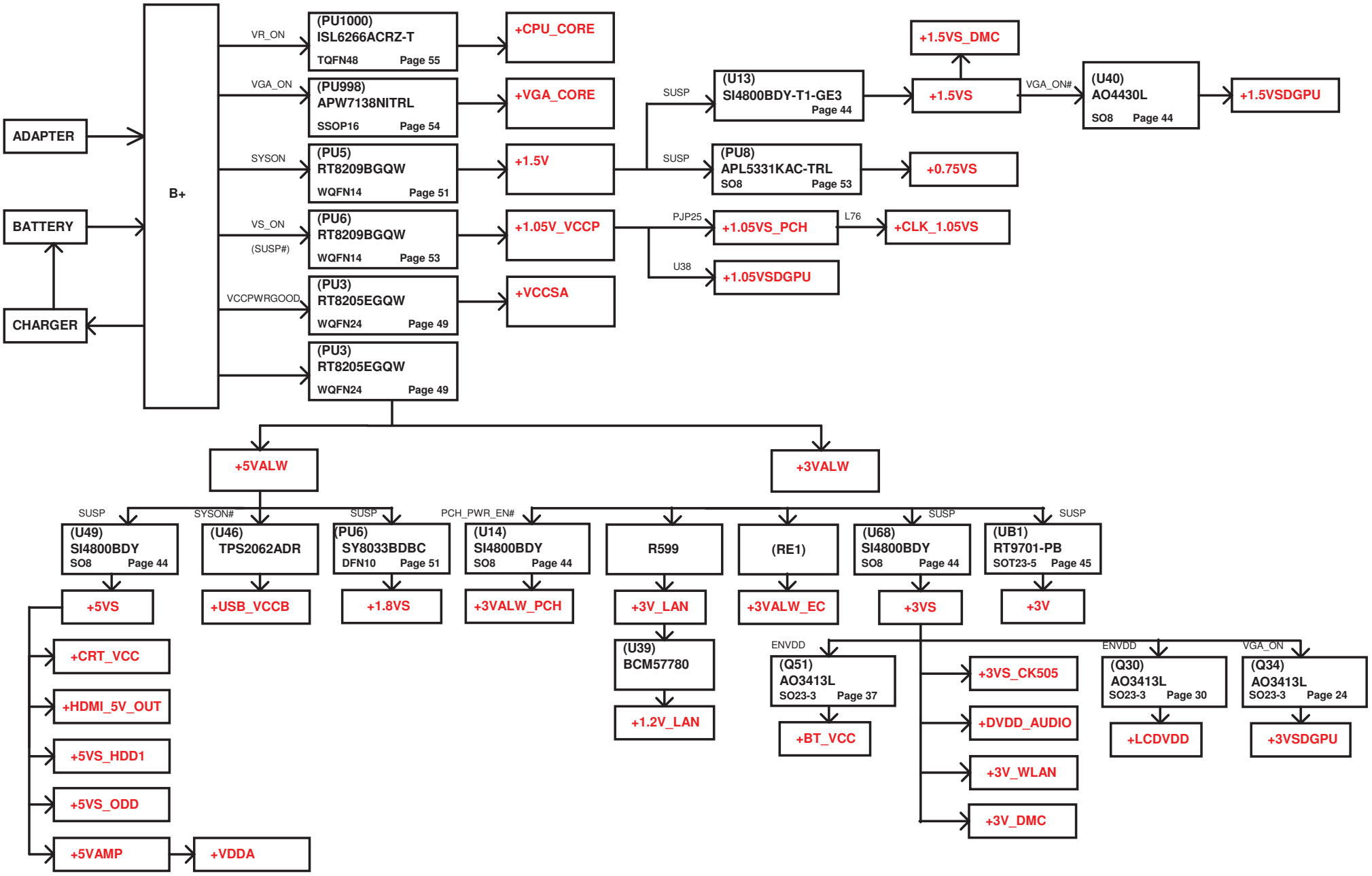
Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
1	Shut down for PWM3 pin floating	IF the PWM3 no used, please pull high it for +5VS and not floating	0.1	P.55	(1)Add PR638(0_0603_5%) between PWM3 and +5VS (2)connect the ISNG to +5VS	2010-03-29	DVT
2	OVP problem with PWR and HW side	If the HW side is 0V, through the jumper will cause the sense pin to over the votage setting and it may happen OVP problem.	0.1	P.55	Change the +VGFX_CORE to +VGFX_COREP	2010-03-29	DVT
3							

COMPAL ELECTRONICS

Title <Title> PIR POWER1

Size A | Document Number PAW00(LA-6361P) | Rev 0.1

Date: Friday, August 27, 2010 | Sheet 55 of 59



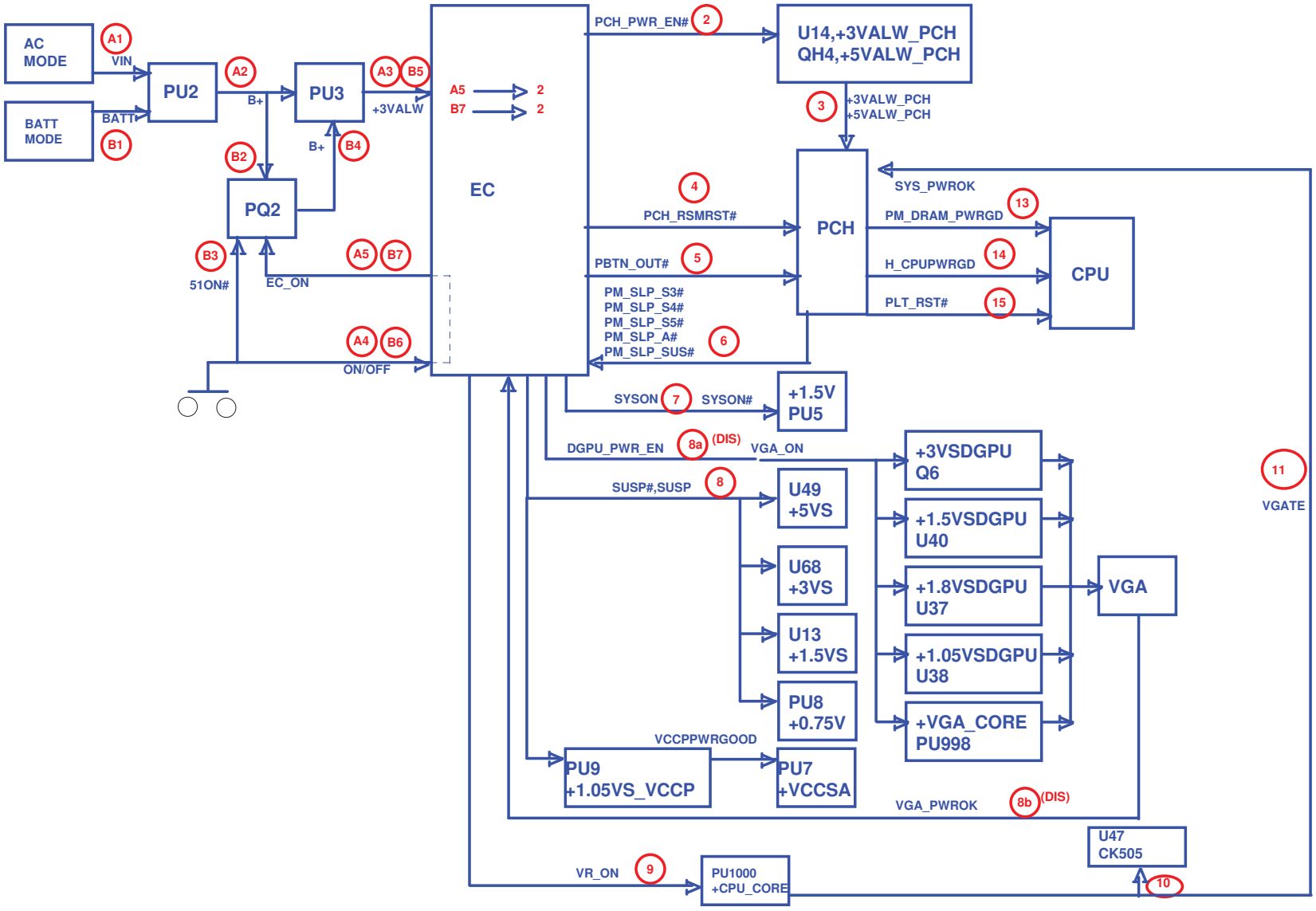
Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: Power Rail

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 56 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: Power sequence

Size	Document Number	Rev
Custom	P5WE0 M/B LA-6901P Schematic	0.1

Date: Friday, August 27, 2010 Sheet 57 of 59

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: EE P.I.R (1)

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 58 of 59

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Security Classification	Compal Secret Data		
Issued Date	2010/08/11	Deciphered Date	2011/08/11

Compal Electronics, Inc.

Title: EE P.I.R (2)

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Friday, August 27, 2010 | Sheet 59 of 59